

Research Needs Document: Nanomanufacturing Materials and Processes

June 11, 2018

Semiconductor Research Corp. (SRC)
Research Triangle Park, NC 27703

Background

This document is prepared to accompany the Call-for-Research in the research program of Nanomanufacturing Materials and Processes (NMP). The research needs in this area are very broad. We present here selected areas of high priorities as identified by our sponsor members.

There is no doubt that nanomanufacturing is getting increasingly difficult. Feature sizes are already 10 nm or less in production; accordingly, research must be directed towards 5-nm node generation and beyond. For lithography, EUV is close to production so opportunities exist for a major paradigm shift. Metrology and defect detection are critical and their effectiveness must be improved in order to ensure that capable solutions exist in a timely and cost-effective manner. For unit processes, new materials are sought after for logic and memory devices. These material options must be paired with manufacturable deposition and patterning techniques. In addition, functional diversification calls for a wide range of other devices, such as required by analog applications and the Internet of Things. For interconnects, the reduced size (thickness and linewidth) introduces additional scattering and at the same time, reliability problems increase. Interlayer dielectrics also experience increasing difficulty in further reducing the dielectric constant. Manufacturing methods and process materials which reduce device and interconnect variability are required.

For an overview, we divide nanomanufacturing into five major groups:

- (1) Patterning
- (2) Front-end processes (FEP)
- (3) Back-end processes (BEP)
- (4) Common areas
- (5) ESH (Environment, Safety, and Health)

It should be noted that the boundary between FEP and BEP is not clearly defined in the industry, due to the increasing kinds of devices fabricated between the semiconductor substrate and the first metal level. Here we simply put FEP as processes for devices of all kinds, including memories, passives, TFTs, sensors, etc., and BEP as those for interconnects and interlayer dielectrics.

Research Needs

The research needs for nanomanufacturing are obviously very wide. In this call, due to limited resources, we have gone through some discussions and identified what our members have considered to be the most critical items for university research. The list of topics within these five groups are shown as follows:

(1) Patterning

- 1a) Resist, patterning, and mechanistic insight for EUV lithography.
- 1b) Directed self-assembly (DSA) using block copolymers (BCPs).
- 1c) Self-aligned patterning processes.
- 1d) Maskless lithography (e.g. e-beam, imprint...).
- 1e) Etch-free feature patterning (i.e., guided or controlled deposition).
- 1f) Pattern transfer, including new material combinations.

(2) Front-End Processes

- 2a) Emerging materials for devices: Chemistry and synthesis (e.g., complex oxides, C-based, novel dielectrics/conductors; for transistors, memories, memory selection devices, etc.).
- 2b) Novel deposition techniques for highly bottom-up thin film growth.
- 2c) Interface/surface physics (SiGe, Ge, Ge-Sn, III/V, contacts, 1-D/2-D materials).
- 2d) Hybrid materials with tunable properties.
- 2e) Material-enabled novel functions.
- 2f) Materials and processes enabling functional diversification on CMOS platform (RF and mm-wave devices, MEMS, sensors, photonics...).

(3) Back-End Processes

- 3a) Cu-based conductor optimization, cap, and barrier layers.
- 3b) Low-k dielectrics and processing.
- 3c) Reliability (electromigration, TDDDB ...).
- 3d) Interconnect contacts and interfaces.
- 3e) Alternate/novel concepts for low-resistance interconnects (beyond-Cu) and novel low-capacitance dielectrics.

(4) Common areas

- 4a) Atomic-layer deposition (ALD), area-selective ALD, and atomic-layer etch (ALE).
- 4b) Area-selective deposition other than ALD. Area-selective deposition of organic films using MLD (Molecular Layer Deposition).
- 4c) Metrology and analytic techniques. 3-D imaging (3-D STEM, atom probe...) and functional imaging (STEM with EELS/EDS, high-resolution strain mapping...). (Note: Collaboration with NIST or other national lab. is highly encouraged.)
- 4d) Modeling/understanding/detection/process control of critical unit processes. Improvement of variability and defects. (Examples: New sensors/techniques for improved process control, imperfections in epitaxial growth, defects formed in liquid solution; Model-based approach that predicts the gap-filling behavior of spin-on materials within high aspect ratio (3-15), sub-16 nm topographic structures, with particular interest allowed for statistical analysis.)
- 4e) Fundamental material and process understandings including new analytical techniques to measure intrinsic parameters such as magnetism, spin, electronic states, and small (sub-5 nm) features.
- 4f) Design for manufacturing (DFM).
- 4g) 3-D monolithic heterogeneous integration.

For Category-5 (ESH), the Research Needs document can be obtained under a separate link in the call announcement.

When submitting the white papers, researchers are asked to indicate the topics (in number) what their research topic can best fit in.

Contributors

Clendenning, Scott	Intel
Cline, Brian	Arm
Felix, Nelson	IBM
Ng, Kwok	SRC
Somervell, Mark	TEL
Torres, Juan	Mentor
Tripp, Marie	Intel
Tsai, Wilman	TSMC