Research Needs Document: Logic and Memory Devices

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Background

This document is prepared to accompany the Call-for-White-Papers for the research program of Logic and Memory Devices (LMD). The research needs in this area are very wide. We present here selected areas of high priorities as identified by our sponsor members.

In an integrated circuit, transistors and memories are the most important and common components. Traditionally, the main goals for scaling are density, performance, and cost. Nowadays, power, both dynamic and static, is one of the most important limiting factors to be addressed at the device level.

A new area in the LMD program is on monolithic heterogeneous 3D integration that will enable greater functionality per footprint including integration of logic and memory as well as mixed-signal circuits, photonics, and spintronics, therefore it has the potential to become a truly multi-functional platform.

For transistors, the push is for devices with lower supply voltage to generate same or higher current per unit channel width as state of the art silicon CMOS..

The natural progression beyond the current manufacturing technologies, SOI planar MOSFETs and FinFETs, will be nanowire MOSFETs, all based on Si channel materials. Other than these Si MOSFET structures, there are potential benefits to be gained by going to alternate channel materials with significantly better transport characteristics than silicon. Low-resistivity contacts to those alternate channel materials are equally critical to low-voltage high performance transistor solutions beyond silicon.

Alternate signal using spin or magnetism as a state variable rather than charge or voltage can avoid resistive power dissipation and is an attractive option. However, the propagation and logic operation based on spin, or conversion of spin back to electrical signal, is a big challenge.

Memories are classified into major categories of nonvolatile memories (NVMs), SRAM, and DRAM. Each has its trade-offs in different aspects of performance, its unique feature and structure, but all are critical to the industry. For NVMs, the industry has been depending on the charge-storage type, which are floating-gate FET and charge-trapping FET. However, both of these devices have a tunnel gate oxide at the channel interface, but due to the stringent requirement of long retention time, this tunnel oxide is already at its minimum thickness and is no longer scalable. Recent products have turned to 3-D to gain vertical space. The industry has started to turn to non-charge-storage types of memory cells that are typically two-terminal. For these NVMs, the critical metrics are write/erase power, multi-bit and density, endurance and reliability, low latency, etc. The leading contenders are MRAM, PCRAM, and RRAM, among others..

These NVM cells typically exhibit *I-V* characteristics that are too conducting at low bias, and provide leakage paths when utilized in x-bar like memory arrays. A selection device is needed in series with the memory element to curtail the leakage from unselected cells. For density and ease of operation, it is desirable to have a selection device that is two-terminal. Selector device challenges include low turn-on voltage, high current density capability in on state, ultra-low current in off-state, and high endurance. .. Ultimately, a NVM cell with built-in selection device is the preferred solution..

Currently the continuing scaling of the 6-transistor SRAM cell and the 1T1C DRAM cell is experiencing formidable challenges. Lower supply voltage, demanded by lower power, causes noise margin issues. Area scaling is another big challenge. Revolutionary device concepts to realize the same functions with fewer device components would be extremely beneficial to the industry.

Research Needs

In this call, due to limited resources, we have identified topics our members have considered the most critical and relevant for university research. The list of topics are shown below, and more-detailed explanation for each follows:

1) Monolithic Heterogeneous 3D Integration using:
    1a) 1D Materials (CNTs & Si-/III-V-based NWs, etc.)
    1b) 2D Materials (Graphene, MoS2, WSe2, etc.)
    1c) High-electron-mobility-transistors a.k.a. HEMTs (GaN, SiC, etc.)
    1d) Next-Generation Spintronic MRAM (Spin-Orbit-Transfer a.k.a. SOT-MRAM)
    1e) C(complementary) FET and 3D integration (e.g. Ge PMOS GAA on Si NMOS FinFET
2) Logic devices:
    2a) MOSFETs with high-mobility channel materials
    2b) Transistors based on tunneling
    2c) Transistors based on non-tunneling transports and phenomena
    2d) Transistors based on spin and magnetism
3) New concepts for contacts, junctions, and gate structures
4) Memories:
    4a) NVM: MRAM
    4b) NVM: RRAM
    4c) NVM: PCRAM
    4d) NVM: FeRAM
    4e) NVM: Other novel concepts
    4f) Analog memories
    4g) Revolutionary SRAM and DRAM concepts
    4h) Metrology for memory devices
5) Selection devices for memory arrays
6) Embedded devices
7) Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena
8) Other topics

1) Monolithic Heterogeneous 3D Integration (MH3D)

Monolithic heterogeneous 3D integration allows higher density packing and integration of logic and memory as well as mixed-signal circuits, photonics, and spintronics, therefore it has significant advantage for the development of multi-functional platform. Currently, significant progress has been made in III-V wafer bonding to 300 mm wafer sizes and hybrid Ge/III-V devices on Si. Looking further ahead, vertical Tunnel FETs, 2D materials and Spintronics are emerging as post-CMOS alternatives while continued scaling is possible with gate-all-around (GAA) and nanowire devices. C(complementary)FET and 3D integration (e.g. Ge PMOS GAA on Si NMOS FinFET) and these possible combinations will be investigated to find the promising CMOS structures. Finally, interconnect technology with low parasitic RC factors and high thermal stability (device formation technology to reduce thermal shock) needs additional research.

2a) Logic devices: MOSFETs with high-mobility channel materials

Many options of materials have been explored: III-V compounds, Si_xGe_{1-x} compounds or pure Ge, graphene, carbon nanotube, TMDs (Transition Metal Dichalcogenides such as $MoSe_2$), other 2-D and 1-D materials and structures, etc. However, the consistent demonstration of high quality channels and gate-stacks, as well as stable low resistance contacts solutions necessary to exceed the state of the art silicon power AND performance capabilities is yet to be achieved on single n and p-type devices.

2b) Logic devices: Transistors based on tunneling

This group of devices shares the attractive feature of steep subthreshold slope beyond the fundamental limit in MOSFETs. There are many device variations in this group. The original version is TFET (Tunnel FET), where the

tunnel current of a *p-n* junction is being modulated by the gate. Other tunneling principles involve bandgap engineering to enhance "On" Current, etc. Some versions invoke tunneling between two layers of materials separated by insulator. Feasibility of NC (Negative Capacitance) FET application for logic (other than FeFET for memory) is still debatable. e.g. the 30nsec measured by pulse P-V to be extended to the real GHz function using Ring Oscillator circuit or the alternative possible method).

2c) Logic devices: Transistors based on non-tunneling transport and phenomena

Novel logic device concepts are sought after beyond the groups 1a and 1b above. There are other kinds of working principles that are unrelated to tunneling.

2d) Logic devices: Transistors based on spin and magnetism

Transistors based on spin and magnetism to some degree. Here we include any device that involves spin and magnetism, even though charge transport as current is in some cases considered an input or output.

3) New concepts for contacts, junctions, and gate structures

New concepts to improve MOSFET structures; parasitic series resistance, abrupt junction formation, high-K/metal gate optimization, etc. Various material tests are needed, especially on silicide.
Strong emphasis on novel high-K materials. This includes NCFET concepts to identify possible candidates and the advantages/disadvantages with the limitation of high frequency operations, and the optimal physical thickness.

4a) NVM: MRAM

All topics related to electrically switched Magnetic RAMs. The leading examples are field free Spin-Orbit-Torque - MRAM (SOT MRAM) by new spin orbital coupling material and field free Voltage-controlled magnetization anisotropy-MRAM (VCMA MRAM). New free/reference-layer materials and device structures (two-terminal) to lower the switching current while maintaining data retention time. New tunnel barrier materials for high magnetoresistance. New capping layer and etching/passivation techniques for improving MTJ stack reliability and yield.

4b) NVM: RRAM

All topics related to Resistive RAM, especially aiming to improve the retention and endurance properties, which are currently the main bottlenecks hindering their industrial adoption. RRAM scope includes (a) OxRAM (Oxide RAM) memory based on motion of oxygen ions and vacancies in an oxide layer ; (b) CBRAM (conductive-bridging RAM) based on the formation of a conductive metal filament; and (c) RRAM development with low power requirements for neuromorphic applications.

4c) NVM: PCRAM

All topics related to phase-change RAM with emphasis on scalable multi-level capabilities.

4d) NVM: FeRAM

NVMs based on ferroelectric materials and effects. All topics related to new dielectric materials and integration schemes with transistors that show high polarization and low coercive field under low thermal budget process. Fundamental understandings of the non-ideality effects (imprint, fatigue and wakeup) and their temperature and film thickness dependence.

4e) NVM: Other novel concepts

Any novel NVM cell concepts different from the groups 3a–3d above.

4f) Analog memories

Nonvolatile memory cells that are capable of continuum equilibrium states. The challenges are controllability and reliability. They provide high density and are especially suitable for neuromorphic computing architectures. Analog nonvolatile memory elements exhibiting symmetric resistance tuning in response to pulsed inputs are particularly attractive. Problems and solutions that may arise when various new memory materials and devices operate as neuromorphic computing memory are also of interest. A systematic methodology to quantify the error tolerance and yields for EDA/design enablement.

4g) Revolutionary SRAM and DRAM concepts
Revolutionary concepts to realize the SRAM or DRAM functions with new materials or simpler device and layout structures. Novel physical mechanisms (beyond charge-based) for fast switching (last level cache type) memories.

4h) Metrology for memory devices
Novel methods and platforms to extract memory device performance and related material characteristics.

5) Selection devices for memory arrays
A critical component for two-terminal NVM cells. Area efficiency is an important consideration in memory cell design.

6) Embedded devices
Logic, memory and interconnect devices embedded in monolithic-3D, back-end-of-line (BEOL), or other beyond-TSV/interposer processes. Novel methodology for enabling these embedded devices co-design with front-end logic transistors.

7) Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena
To help advancement in logic and memory devices, the use of numerical simulation is often required. In this area, we solicit ideas for improvements in modeling capabilities and in developing computationally efficient methods for materials, processes, and device operation. Use of these tools to study new material properties, unit processes, device behaviors, and quantum phenomena arising from nano-scale geometries is of high interest. The efforts to perform large-scale design technology co-optimization (DTCO), and to build multi-physics/domain simulation methodology are highly encouraged. Finally, technology for reliability analysis (simulation/modeling) is needed.

8) Other topics
Outside the six focus areas above, all submissions will be considered if containing outstanding, out-of-the-box ideas.

Reliability is a topic of interest for both logic and memory devices. Proposals addressing reliability issues pertaining to a specific device (especially emerging memories) should be submitted to the group of the device type.

In this call, we encourage innovative ideas that are impactful to the semiconductor industry. Proposed work of high-risk and high-reward is especially suitable for university research.

When submitting the white papers, researchers are asked to indicate the topics (in number and sub-category such as 1c) that their research topic can best fit into.

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