Research Challenges in Computer-Aided Design and Test
June 2019

The Computer-Aided Design and Test (CADT) research program at the Semiconductor Research Corporation (SRC) is soliciting university proposals to address challenges facing the industry. These challenges have been developed by experts in SRC member companies and they have indicated that machine learning techniques, applied to the challenges, are of keen interest but not necessarily required in successful submissions. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

This document has four major sections:

- Functional Safety Tools and Techniques
- System, Logic, and Physical Design Tools (SLPD)
- Test
- Verification

New emphasis on functional safety is described in this document as that has risen in prominence with the increased use of electronics in automobiles and industrial applications. This topic may be considered to be a cross-cut to the other need topics in CADT: SLPD, Test, and Verification.

SRC seeks university research which is pre-competitive, and promotes interaction between faculty and industry to address challenges that members see in future systems and technologies. Unfortunately, only a very small number of proposals will be selected for funding.

Be sure to follow the instructions in the Request for Research when responding.

Note: the following needs are not listed in an organized priority ordering.

Contributing members include Arm, IBM, Intel, Mentor, NXP, and TI.

Functional Safety Tools and Techniques

F1 Safe System

This subject summarizes the interests of member companies on tackling the safety of a system from its high-level modeling all the way down to the suitable fault models of devices aiming field failures. It covers the wide range of desired methods to model a complicated system, to perform safety analysis of the system, to perform fault injection to report diagnosis coverage, to enable fault simulation at different design abstraction levels and relate coverage across those levels, and to select effective in-field test and safety mechanism. Methods to approach safety analysis in a holistic and automated way which could cover different level of system hierarchy and complexities are very important in the space of functional safety.

F1.1	Fault models in the context of functional safety that address latent defects, aging, and other physical and electrical disturbances in the field
F1.2.	Methods to model, simulate, validate and test a safe system, especially large system with emerging (machine learning) accelerators
F1.3	Methods of fault injection and fault simulation for safety metrics evaluation against safety goals and effective methods to model and simulate faults in analog and mixed-signal circuits
F1.4	Methods to select and deliver effective in-field test and diagnostic stimuli

F2 Data Mining and Failure Prediction

Automotive industry maintains a good field failure return mechanism which allows the member companies to analyze the failures to improve quality assurance and/or to enhance design robustness. The field failures can also become invaluable in obtaining deep understanding in the failure mechanisms, mission profiles, and effectiveness of the safety mechanisms. In turn, the knowledge gained through field failure analysis can be applied to predict the probability of failures over the device's lifetime which becomes critical in autonomous driving era. The member companies are asking researchers to come up with effective methods to analyze the field failure data through preferably machine learning techniques and apply the knowledge to enable failure prediction over device's lifetime. Automated methods to perform real-time analysis of in-field degradation in order to detect and communicate imminent failure is needed. Getting access to the data will be one of the most daunting tasks for the researchers, creating an effective collaboration model with convincing plans and/or demonstrated history is highly valued.

F2.1	Methods assisted by machine learning to collect and analyze field data for safety analysis
F2.2	Methods of failure prediction assisted with aging and reliability model as well as system history

F3 Design for Functional Safety

To ensure system safety, a top-down safety analysis from OEM to IP level is the state-of-the-art method to drive system architecture definition, safety mechanism addition/removal. The IPs available today often time cannot provide the adequate information e.g. diagnostic coverage or built-in safety mechanisms that are needed to reach system-level safety goal. Designing IPs with architectures/topologies as safety element out of context and/or designing infrastructures to allow

inter-chip on-line testing and diagnosis are of great interest of member companies. Automated methods can assess and comprehend component vulnerabilities to design and synthesize robust systems.	
F3.1	The design automation of architectures of digital, memory, clock, power management and data converters designed to enable those IPs as Safety Element out of Context (SEooC)
F3.2	The design automation of inter-chip infrastructure to enable safety mechanisms to cover I/O, pad-ring, packaging failures
F3.3	The design automation to help design self-checking functional test patterns to achieve sufficient diagnostic coverage
System, Logic, and Physical Design Tools	
S1 System Tools: Key Design Goals – Power Efficient High-Performance Designs, Long Term Reliability	
S1.1	Tools for system-level analysis and design. This includes, but not limited to: • Techniques for systems that functions across broad range of performance • Tools and methodologies to address reliability and robustness for power efficient high-performance designs • Techniques to evaluate and implement adaptive self-test design methods for use at the time of manufacture as well as in-field, to aid in diagnosis, isolation, and repair
S1.2	Planning, exploration, and design tools for homogeneous/heterogeneous multi-core systems, including innovative and efficient communication fabrics, clock distribution, etc.
S1.3	Logic/physical/high-level synthesis and cross-boundary optimization. Cross-level optimization tools that can propagate physical implementation details up to the system level. This topic includes, but is not limited to • 3D design flow tools and trade-off analyses including synthesis, floor-planning, placement, power delivery, clock-tree synthesis, routing, DFT, thermal analysis, etc. • Predicting the electrical performance impact of mechanical stress
S2 Tools for Design Robustness	
S2.1	Tools to reduce the design margin from timing and reliability guard bands between sign-off and silicon. Tools and optimizations for accurate performance, power, and reliability margins of analog, digital and mixed-signal designs at functional and physical levels for automotive (high reliability & high yield) and low power designs
S2.2	Tools and optimizations to reduce infant mortality, to comprehend in-field degradation mechanisms like aging to achieve graceful failure, or to improve reliability against aging effects
S3 Analog Tools	
S3.1	Tools for analog DFM that focus on critical devices (matched pairs, current mirrors, etc.) and minimize unaccounted exposure to random and systematic variations (e.g., layout dependent effects)
S3.2	Tools for modeling and automation of design of multiple passives (MEMS, inductors, capacitors) as well as sensors

S3.3	Advanced simulation tools for analog design including sensitivity to latent and hard defects or aging effects
S3.4	Analog synthesis and optimization, taking into account designer intent
Test	
T1 Test of Machine Learning Systems	
T1.1	HW and SW methods to evaluate correctness of on-line and off-line learning to ensure continued acceptable performance for learning/prediction during real-time application in the field
T1.2	Data sets for test and validation of learning system before deployment
T1.3	Metrics for correctness and acceptably correct inference
T2 Test Cost, Quality, and Yield Improvement	
T2.1	Reducing the cost of test through various means including adaptive test, burn-in elimination
T2.2	Novel design-for-defect-tolerance methods
T2.3	Methods and metrics to expose and isolate subtle defects and marginalities in digital and mixed-signal systems
T3 High-Level Test, Validation, Diagnosis and Repair	
T3.1	System-level test and in-system debug
T3.2	Bridging pre-silicon to post-silicon verification
T4 Analog, Mixed-Signal, RF, and High-Speed Test	
T4.1	DFT methods, including BIST and BIT, with coverage and test metrics to detect defects/marginalities in analog, high speed, I/O, sensors and RF circuits and systems
T4.2	Accelerate methods to obtain defect coverage for analog/mixed-signal circuits
Verification	
V1 Verification of Machine-Learning Systems	
V1.1	Formal and semiformal approaches to verification of machine learning systems including defining metrics, establishing confidence, and showing transparency in decisions making
V1.2	Approaches to bound behavior for ML systems, especially those that are adaptive in nature
V2 Machine Learning Techniques for Verification	
V2.1	Learning algorithms for specification and verification of digital and AMS systems
V2.2	Learning algorithms targeted at efficient functional verification, debug, triage, and coverage closure
V2.3	Learning algorithms for better post-Si debug

V3 System-Level Verification	
V3.1	Formal and semi-formal methods applied to security and emerging applications
V3.2	Scalability of dynamic verification techniques
V3.3	Techniques to assess and verify system functionality/resilience in the presence of soft or hard errors
V3.4	Efficient verification of SoC, platform, and system level non-functional properties, especially power, performance, security, and safety
V3.5	Co-verification of systems containing hardware and software/firmware components
V4 Formal Technologies for Specification, Design, and Verification	
V4.1	Improved analog/mixed-signal specification, verification, equivalence checking, regressions, and coverage analysis
V4.2	Improved scalability and functionality of core technologies including automated model checking, solvers, synthesis for verification, and security verification
V4.3	Formal techniques for comprehensive component interface and system integration functional specifications
V4.4	Agile/incremental verification techniques that tightly integrated with agile/incremental design
V4.5	Techniques to enable provably-correct system integration or correct-by-construction