Semiconductor Research Corporation

July 23, 2021 Workshop at SRC

ASCEND: American Strength in Semiconductor Chips for the Economy and National Defense

Growing for decades, there is now a critical imperative to design and create a national capability for advanced packaging technology (APT) and to reinforce the R&D infrastructure for domestic microelectronics

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Executive Summary

Growing for decades, there is now a critical imperative to design and create a national capability for advanced packaging technology (APT) and reinforce the Applied Research and Development pipeline for domestic microelectronics. With the imminent demise of two-dimensional geometric scaling as the driver of Moore's Law economics, the microelectronics community has converged on APT as the key approach for maintaining the performance gains experienced over the past four decades and that the world will need for decades to come. At the same time, we cannot simply pivot from microelectronics to APT or we risk squandering our existing lead in microelectronics. The stakes are high because the country that dominates both technologies will control the economics of microelectronics manufacturing, ensure national security for their electronic systems, including defense, and manage the microelectronics supply chain that feeds trillions in global GDP growth. In response to this national imperative, SRC recently convened an in-person workshop with leaders from industry, including AMD, IBM, Intel, NXP, and Texas Instruments along with academic leaders in microelectronics and APT including Purdue, SUNY Binghamton, and Georgia Tech. The goal of the workshop was to develop a strategy and actionable plan. In this paper, we recommend that SRC design a large-scale Microelectronics Manufacturing USA Institute (MMUSAI) for US manufacturing of both microelectronics and advanced packaging technologies (MAPT). This large-scale MMUSAI will create new domestic capabilities and will fill the large gap in the US innovation pipeline while creating domestic manufacturing jobs. With this paper, we invite the US Government, specifically the Department of Commerce, to join us in this quest.

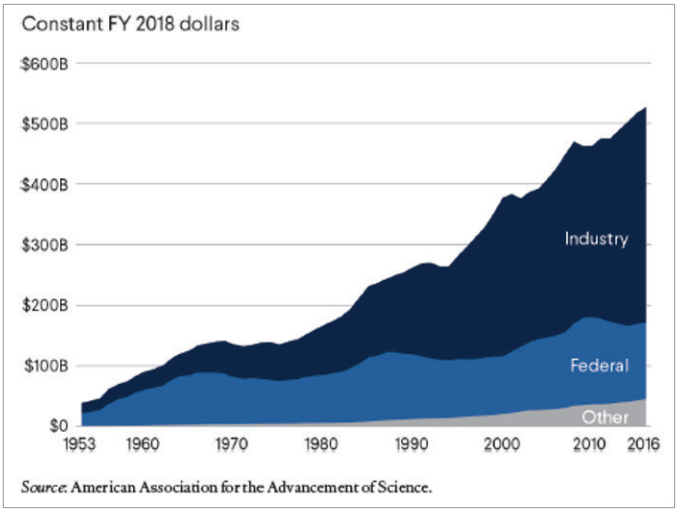
Introduction

Over the past several decades, the microelectronics industry has changed the way we work, play, and connect, while also enabling trillions of dollars in economic prosperity and transforming our national security. During this time, however, the industry fractured into specialized regional supply chain blocks. While each of these specialized blocks has different economic and risk characteristics, together they deliver a system that supports massive industrial growth. The resulting global supply chain is highly optimized to convert silicon ingots into integrated circuits that meet and drive consumers' needs.

Regional hubs represent the greatest risk to US economic and national security. The global supply chain has consistently supplied US companies with access to the latest technologies and has served US companies well regarding cost and delivery. But this comes at the expense of risks posed from geopolitical conflict, dramatic weather events, regional economic instabilities, and even the current pandemic. Specifically, although US companies account for over 50% of the revenue in the microelectronics industry by dominating IDM and Fabless/Design, much of the manufacturing capacity is overseas, which has led to a reduction in US manufacturing capacity from 37% in 1990 to 12% in 2020.

Putting the US at further risk is our forfeit of leadership in manufacturing leading technology nodes. We are now one to two technology nodes behind global leaders in Asia. This brings significant economic risk, but it poses an even greater national security risk. Without access to the most advanced technology nodes, we cannot expect national defense to reach its goal of overmatching potential threats. Fueling this, GlobalFoundries recently announced that they would not continue the pursuit of advanced technology nodes, and Intel is now one to two nodes behind global leaders Samsung and TSMC. Countering this, Samsung and TSMC's growing commitment to microelectronics manufacturing facilities in the US is a welcome source of capability.

Part of the reason that the US has fallen behind in technology nodes and has steadily decreased domestic manufacturing capabilities is because of the R&D spend by competing governments. US federal investment in R&D as a percentage of GDP peaked at 1.86% in 1964 but has declined, moving from a little over 1% in 1990 to 0.66% in 2016. As a percentage of the budget, federal R&D peaked at close to 12% in the mid-1960s because of the Apollo space program but declined in the following years, dropping to nearly 3% in 2017. This has conceded the technology advantage to other nations, allowing them to lead in these areas and translate that technical leadership into technical dominance. Figure 1 illustrates the reduction in US spending on R&D by the US government, as well as the rapid acceleration of China's spend on R&D and workforce development. We must develop the technology, the systems to create the technology, and the talent for the US and its allies to lead in microelectronics for the future.



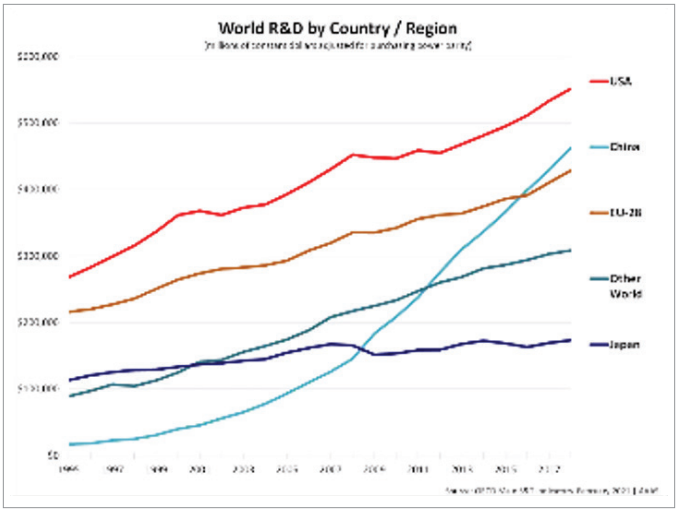


Figure 1. The US Government must increase investments in microelectronics to remain globally competitive.

The Three Problems That Need to be Solved

1. The Lab to Fab Pipeline has gaps.

To ensure the US has access to secure, high-performance microelectronics we must have a domestic and robust innovation pipeline from ideation through manufacturing, or 'Lab to Fab' as it's sometimes called. While the microelectronics innovation pipeline is strong in many areas domestically, it does have vulnerabilities in key areas. Furthermore, there are urgent opportunities to dominate microelectronics technology and manufacturing by establishing new domestic capabilities in these gaps.

Specifically, the Lab to Fab pipeline can be divided into four pillars with each pillar feeding subsequent pillars as illustrated in figure 2. The pipeline starts with Basic Research, where exploration and discovery lead to new concepts and fundamental breakthroughs in our knowledge. This doesn't have direct market application but expands our understanding. Discoveries in Basic Research are used by Applied Researchers to create and test ideas that could become solutions for our world. Once tested, these Applied Research concepts can be matured further into Development towards real-world applications. From there, the technologies can be demonstrated, proven effective in piloting, and scaled for manufacturing.

The US has a strong Basic Research capability supported by our NIST Labs, DOE National Labs, NSF, and academia. The Applied Research capabilities for microelectronics is reasonably established but needs continued nurturing to remain globally competitive. Microelectronics and Advanced Packaging Technology (MAPT) in Applied Research exists in several forward-looking universities and industry labs, including Purdue, SUNY Binghamton, and Georgia Tech. However, to meet the needs of economic and national security there is a need and opportunity to grow APT capabilities by 10-100X. This is also true for the Development pillar of APT. While Demo & Scale exists, further evolution would ensure that technologies created in the Applied Research and Development pillars don't get lost in the Valley of Death before they can be moved into manufacturing. See the illustration on the following page.

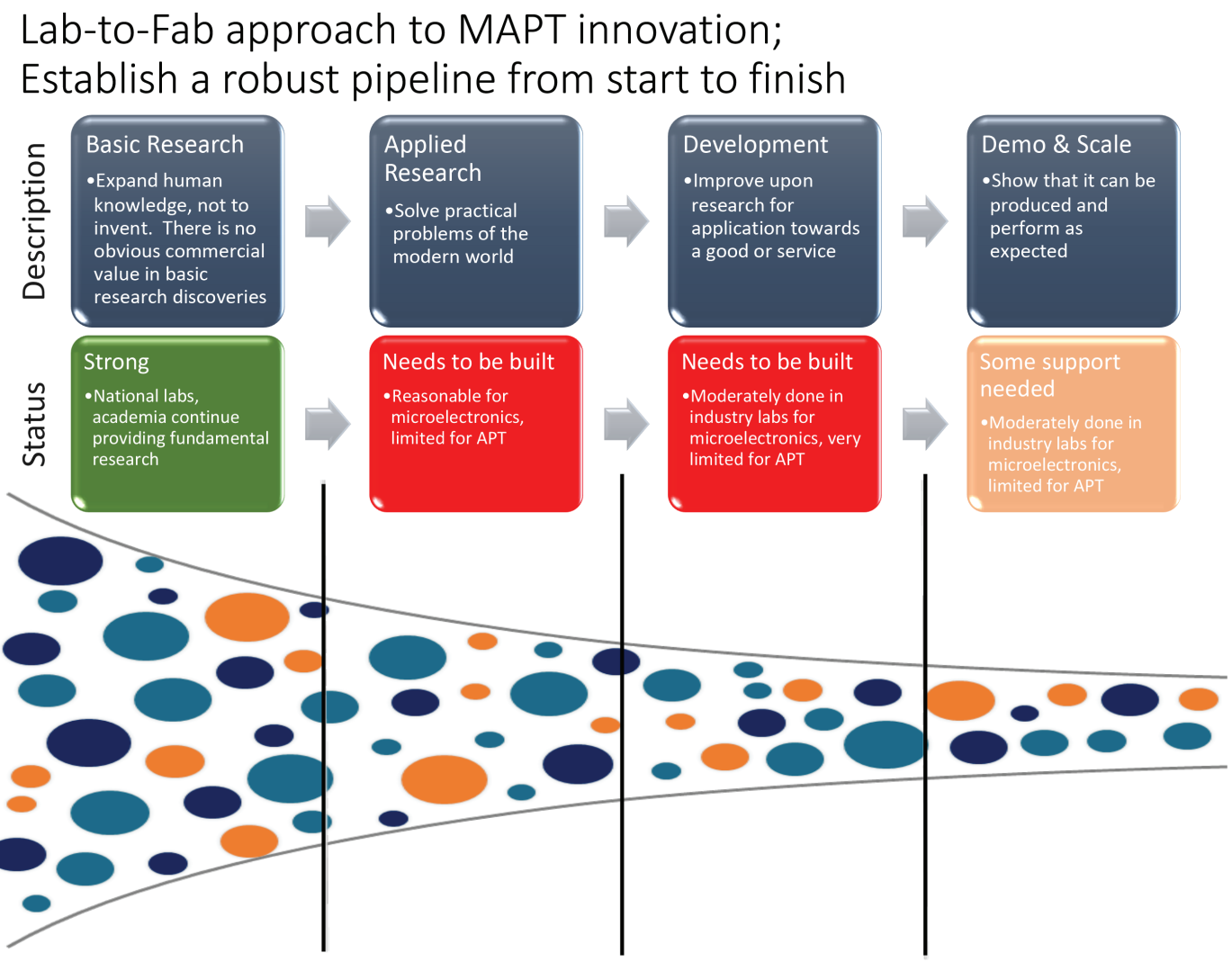
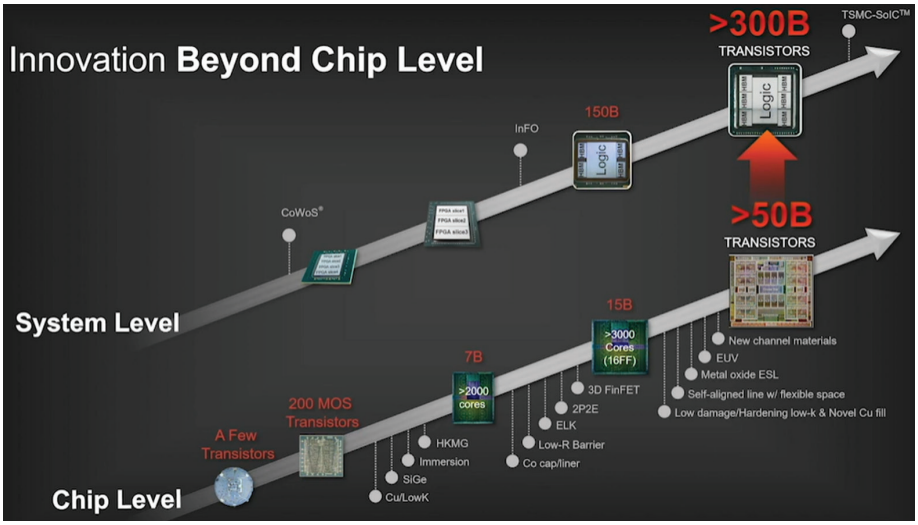


Figure 2. Current description and status of US innovation pipeline for microelectronics and advanced packaging technologies (MAPT).

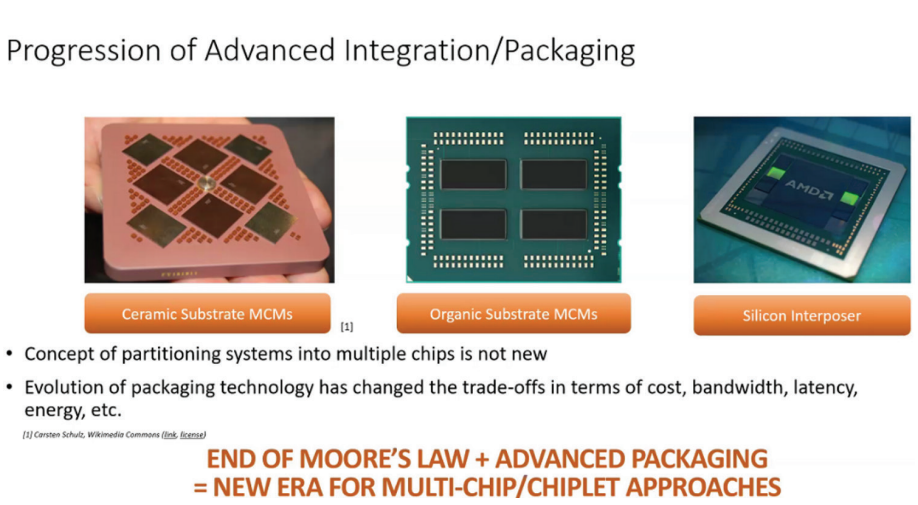
2. The future of economic prosperity and national security will be determined by leadership in APT as well as microelectronic technologies.

Further evidence that these topics need infrastructure support and a national capability to be created is that industry titans have long recognized the ultimate end of Moore's Law from atomic limits associated with two-dimensional geometric scaling and are now pointing to APT as the near-term solution. This will drive continued performance gains, highlighting a pressing need to invest in microelectronics for the next wave of chipmaking advances based on three-dimensional chips and newly integrated functions (embedded memory, communications, novel architectures). Whichever country wins this race, wins the technology future. For example, Dr. Mark Liu of TSMC highlighted this point during his ISSCC 2021 plenary talk, illustrating that TSMC's commitment to both monolithic integration and advances in cutting-edge chipmaking were one part of their continued success story. In addition, Liu continued, is their commitment to advanced packaging technologies, such as CoWoS, Info, and TSMC-SoIC, which has been the primary driver of system-level advances that deliver the requirements for end customers and growing markets. AMD, who is now using TSMC to manufacture

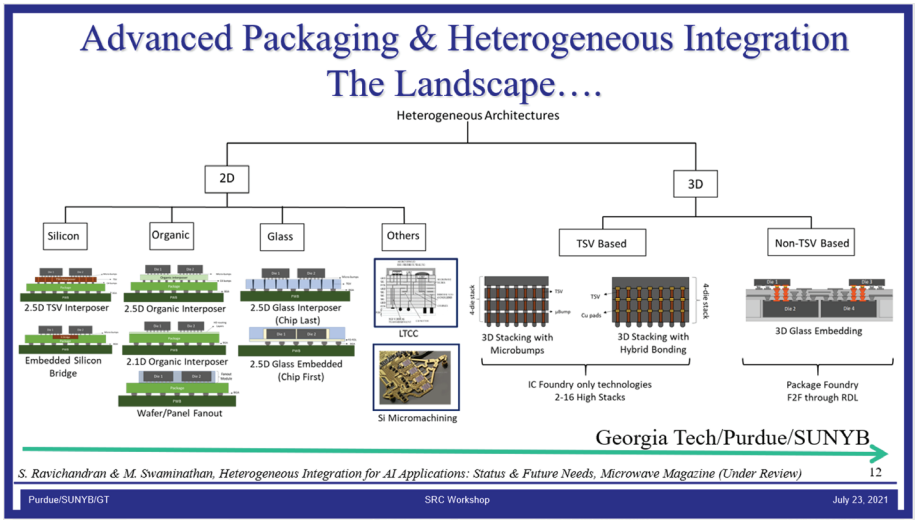
their cutting-edge chips, is evaluating both architectural and integration options based on TSMC's APT innovations. The following four examples, three of which are from the July 23rd SRC workshop, illustrate these critical points:



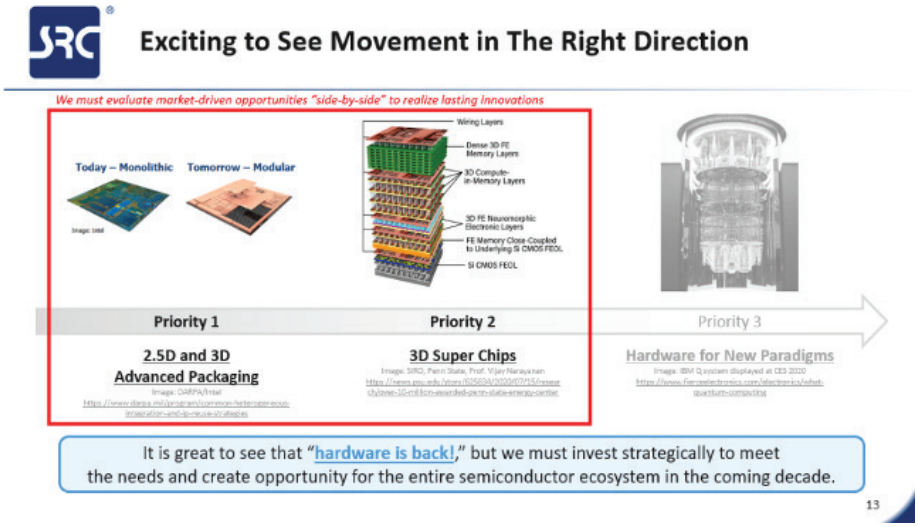
At ISSCC-2021, Dr. Mark Liu's plenary talk highlighted the importance of driving both microelectronics and advanced packaging technologies (MAPT) to achieve both the chip-level and system-level improvements required by cutting edge technologies. TSMC is the world leader in both domains.



At the July 23rd SRC workshop, Dr. Steve Kosonocky, Senior Fellow at AMD, provided an industrial R&D perspective, noting that advanced packaging technologies (APT) and new compute and communication architectures driven by APT are now the primary value drivers for ICT innovation.



At the July 23rd SRC workshop, Prof. Madhavan Swaminathan of Georgia Tech, illustrated how Purdue, Georgia Tech, and SUNY-Binghamton, are global thought leaders in advanced packaging technologies (APT), including 2.5 and 3D technologies with and without through-silicon vias (TSVs). This includes various substrates and interposers (silicon, organic, glass, etc.)



At the July 23rd SRC workshop, SRC's Chief Scientist, Dr. Victor Zhirnov stressed the importance of investing strategically in both 2.5 and 3D advanced packaging technologies as well as continued investment in 3D ICs that enable heterogeneous integration and new functionalities in future chips. MAPT includes the nation's top two priorities.

Industry leaders agree that the continuation of Moore's Law performance gains through APT is the primary solution to the atomic limits of geometric scaling while we continue to invest in chipmaking of 3D integrated circuits, or 3D ICs.

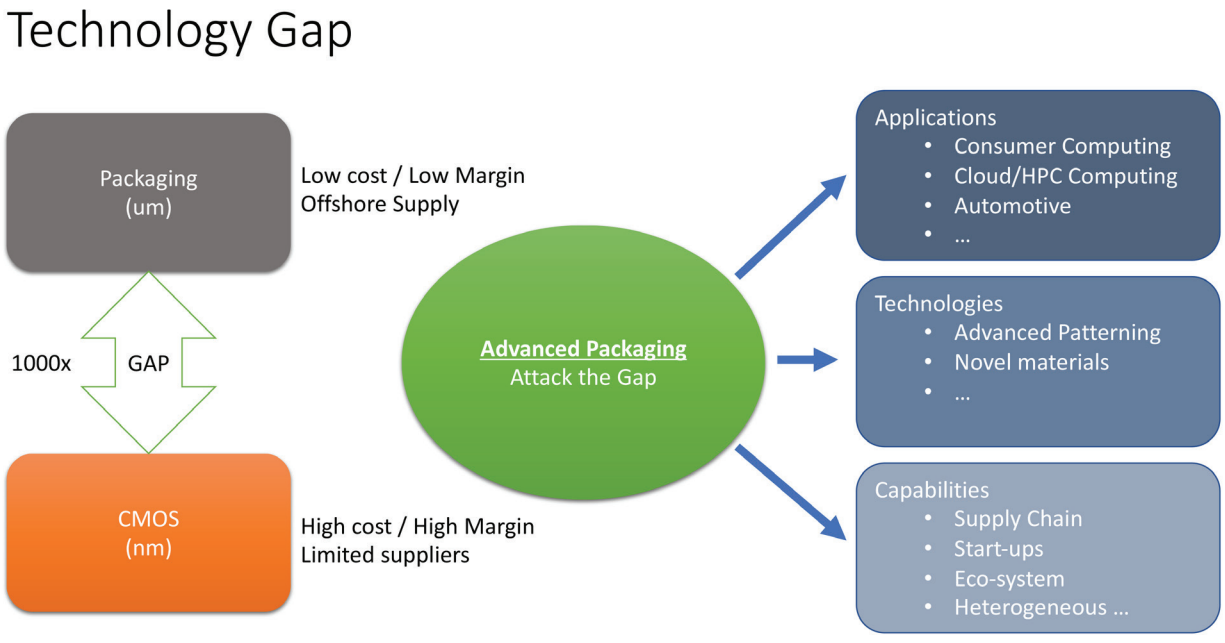
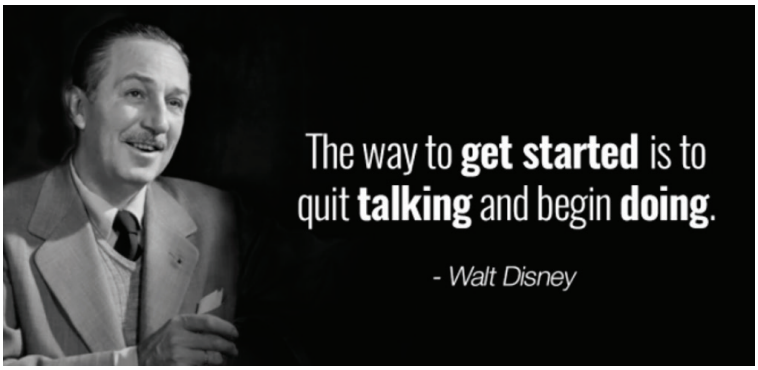


Figure 3. Advanced packaging technologies (APT) attack the 1000x dimensional gap between microelectronics and traditional packaging methods. APT will drive system innovations in 2025+.

To make this a complete and comprehensive portion of the MMUSAI it must include not just Heterogeneous Integration and 3D ICs but must also include advanced packaging for opto-electronics, power electronics, and other packaging strategies. In doing so, it will meet the rigorous thermal, mechanical, and performance specifications for the demands of new market opportunities in high performance computing (HPC), edge computing, automotive, wireless communications, space/defense, and personalized healthcare.

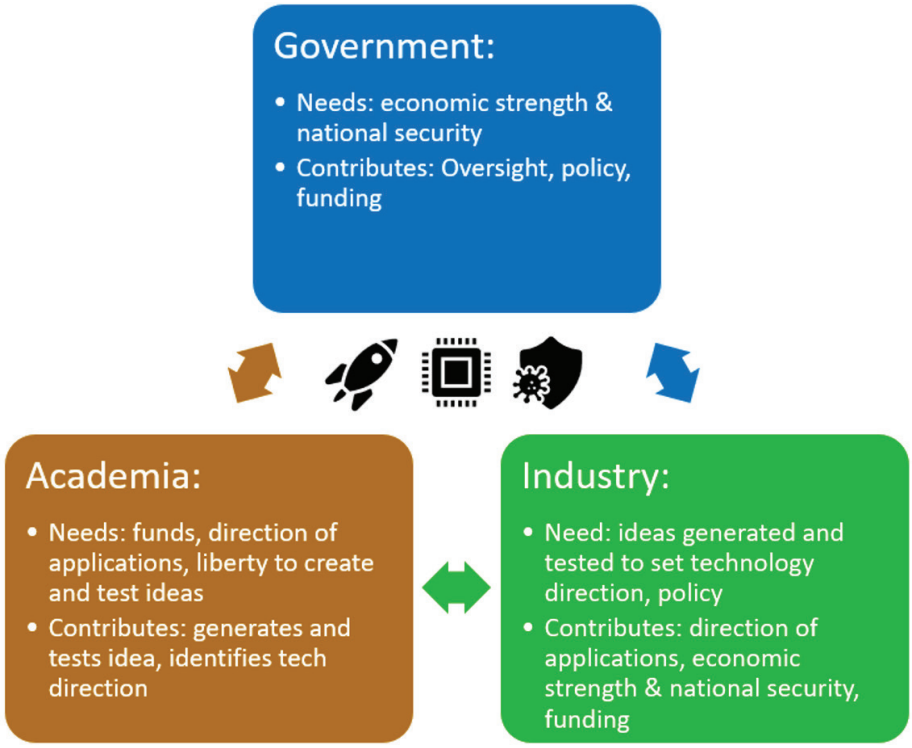
3. We must begin doing.



The third problem to solve is not technical but systematic and the impending urgency to act. Many of the problems we're trying to solve, and our approach to solving are outlined in many recently published reports and papers. This workshop report is not meant to contradict or replace any of these but rather, this paper is meant to take the recommendations of the What, How, Why and roll it into an actionable plan that can begin today. At this point the problems have been studied, congress has introduced legislation, but now is the time to put it all into action before we *study* our way into further economic and national security risks. Below lists recent publications describing the need for this plan:

1. **SRC Decadal Plan (2021)** https://www.src.org/about/decadal-plan/
2. **Heterogeneous Integration Roadmap (2021)** https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html
3. **100 Day Supply Chain Report (2021)** https://www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf
4. **SIA Strengthening the Global Supply Chain in and Uncertain Era (2021)** https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf
5. **NDIA: How to On-Shore Critical Semiconductor Production, Secure the Supply Chain, and Provide Access for the Industry Base (Feb. 2021)** https://www.ndia.org/-/media/sites/ndia/divisions/electronics/images---resources/ndia-on-shore-semiconductor-products-supply-chain-and-industrial-base-white-paper-final.ashx
6. **ITIF Report: An Allied Approach to Semiconductor Leadership (2020)** https://itif.org/publications/2020/09/17/allied-approach-semiconductor-leadership
7. **SIA Sparking Innovation 2020: How Federal Investment in Semiconductor R&D Spurs U.S. Economic Growth and Job Creation (2020)** https://www.semiconductors.org/wp-content/uploads/2020/06/SIA_Sparking-Innovation2020.pdf
8. **Semiconductors: US industry, Global Competition, and Federal Policy by Congressional Research Services (2020)** https://crsreports.congress.gov/product/pdf/R/R46581
9. **Council on Foreign Relations Independent Task Force Report 77: Innovation and National Security; Keeping our Edge (2019)** https://www.cfr.org/report/keeping-our-edge/pdf/TFR_Innovation_Strategy.pdf
10. **SIA Blueprint- Winning the Future (2019)** https://www.semiconductors.org/wp-content/uploads/2019/04/SIA_Winning-the-Future_Refresh_FINAL1.pdf
11. **CARTS: Consortia Analysis and Recommendations Trade Study by Potomac Institute for Policy Studies (2018)** https://potomacinstitute.org/images/studies/CARTSsm.pdf
12. **DOE Office of Science Basic Needs in Microelectronics Report (2018)** https://science.osti.gov/-/media/bes/pdf/reports/2019/BRN_Microelectronics_rpt.pdf
13. **PCAST: Ensuring Long-Term US Leadership in Semiconductors (2017)** https://obamawhitehouse.archives.gov/sites/default/files/microsites/ostp/PCAST/pcast_ensuring_long-term_us_leadership_in_semiconductors.pdf

A Strategy for Solving These Problems



The approach we propose is not unique, but rather a time tested and proven approach to solving monumental national challenges. America has achieved monumental challenges by pulling the three stalwarts of the nation's economy, including Industry, Government, and Academia together to achieve them. Examples include space travel to put mankind on the moon, building the microelectronics industry to usher in the electronics era, vaccinations from polio and smallpox to COVID-19, and the internet. This only works when all resources are aligned and committed. To meet this challenge government, industry, and academia must act together as a system, and the system must be set up such that each partner contributes and benefits according to their needs and attributes. Government must be an active partner to catalyze the launch and creation with policy, funding, and direction. Once created, government funding can be minimized but oversight should remain while the system lives in perpetuity.

In this case, the monumental challenge includes creating new national capabilities that fill the gaps outlined above. Many pieces of this already exist, but with weakness and gaps in the pipeline the US is susceptible to risks from international suppliers that often have their interests misaligned with the US. Specifically, we need to address each of the pillars in the innovation pipeline as follows:

1. Continue to nurture fundamental discoveries through investments in NIST Labs, NSF, DOE Labs, and academia.
2. Build a new national capability of resources and infrastructure in both Applied Research and in Development for APT while continuing to foster microelectronic research that ensures global leadership.
3. Expand support for Demonstrations and Scale to ensure transition to manufacturing.

This strategy requires that much of the Applied Research be performed by academia, guided and accelerated by industry, managed by SRC, and overseen by government. In addition to supplying industry with technology this also will provide critical intelligence to policymakers and provide them with technical solutions which enable desirable policy. That is, policy can't be written and enacted without technical feasibility. We must keep policymakers informed of what is possible, what is not probable, and what can and will become possible so realistic policy can be written to favor US interests.

Addressing these needs will have the following results:

- This will secure the economy by minimizing supply chain risks and catalyzing prosperity
    - This will eliminate the current risks associated with manufacturing advanced performance and advanced technology node microelectronics solely in Taiwan and Korea, which is subject to geo-political influences
- This will strengthen national security
    - By ensuring access to leading performance technology and trusted & assured microelectronics for the warfighter
    - By ensuring trusted packaged microelectronics for the financial systems, for transportation and energy distribution systems, and for consumer products and data
- This will create US manufacturing jobs
    - Developing systems and infrastructure for researching, creating, and developing advanced technology will determine what is manufactured.
    - By creating the tech on-shore we're better able to capture the manufacturing of that technology on-shore.

Ultimately, this becomes a virtuous cycle where manufacturing, academia, workforce development, and next-generation technology feed each other.

To solve these problems, we will stand up capabilities that can adapt and be relevant in the future while also being complementary to concepts being proposed by congress. When looking at all of these concepts in both the House and Senate bills together and considering how they fit, figure 5 shows how a robust and comprehensive innovation pipeline can be built for both microelectronics and advanced packaging technologies (MAPT).

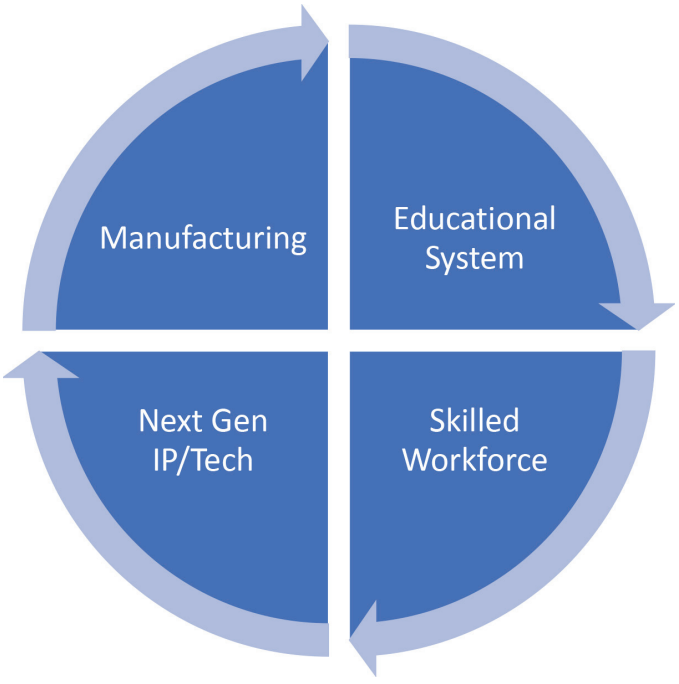


Figure 4. Objectives of MMUSAI for building innovation pipeline infrastructure

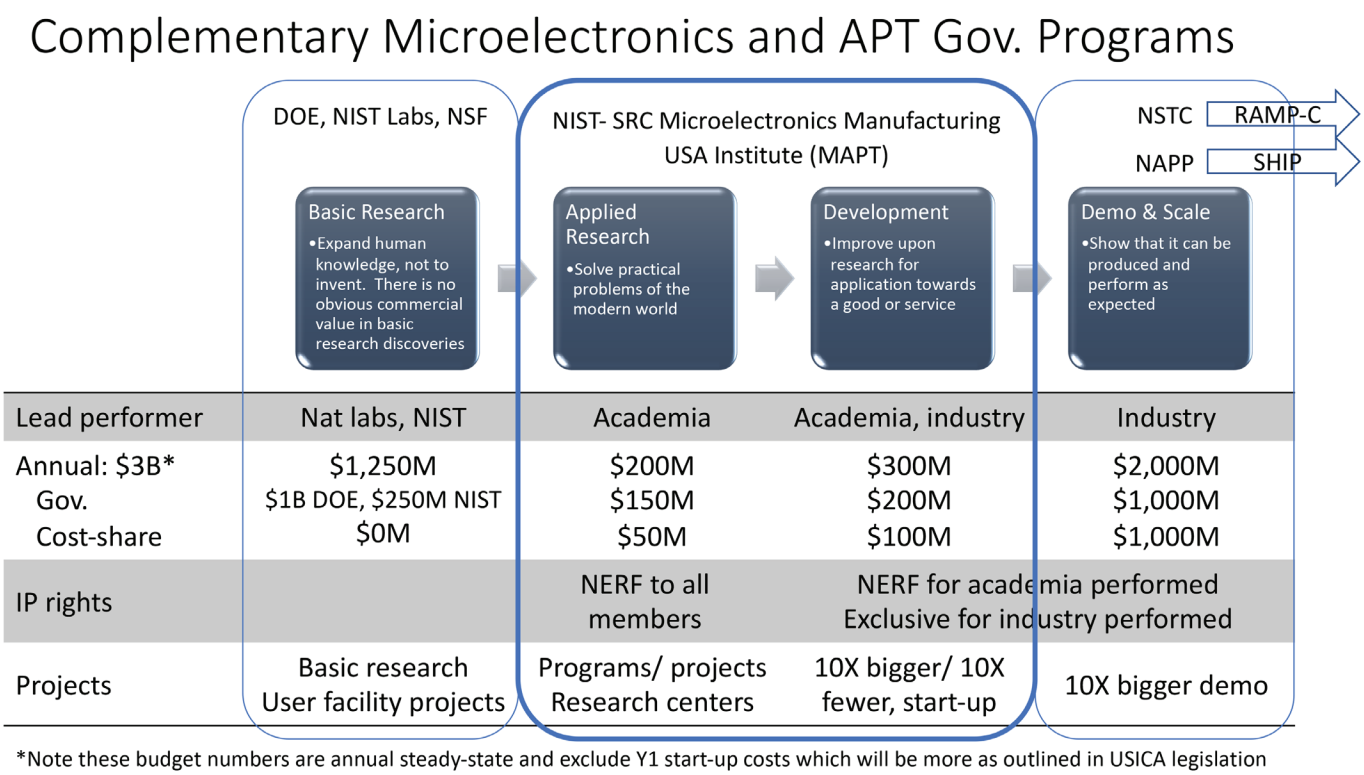


Figure 5. Illustration of how complementary microelectronics and APT government programs aligned with USICA and House bills' programs

The scope of SRC's role would be to develop infrastructure that fills the gaps for a robust pipeline of innovation from ideation through manufacturing. The Basic Research and Demo & Scale pillars of the pipeline need continued nurturing, but this is outside of the scope of SRC's charter. Instead, SRC and our members believe that we should take a leadership role in fortifying the Applied Research and the Development pillars of the pipeline. To do this, SRC must create a large-scale NIST- SRC Microelectronics Manufacturing USA Institute (MMUSAI).

The MMUSAI will include:

1. Applied Research

   a. APT: Building academic research infrastructure in Advanced Packaging Technology (APT) beyond the 8 U.S. universities currently doing it in industry-relevant ways.

   b. Microelectronics: Continue nurturing the US academic microelectronics research infrastructure to ensure global leadership.

   c. Together, they make MAPT, or Microelectronics and Advanced Packaging Technologies.

2. Development

   a. Industry and Academia perform R&D together to create industry-relevant technology and to transfer Applied Research into industry labs with minimal friction.

   b. Supply technology into NSTC and NAPP centers of excellence which feed into programs such as RAMP/RAMP-C and SHIP.

3. Build the workforce through DE&I, training, and workforce development in AA, BS, MS, PhD
4. Ensure tech transfer into industry labs and sharing of industry best known methods with academia
5. Create standards and benchmarking where needed to evaluate competing strategies and rally around meaningful solutions.

This must be done in a framework where we stand up new capabilities that can adapt and be relevant in the future. Below illustrates how the Applied Research and the Development pillars fit together.

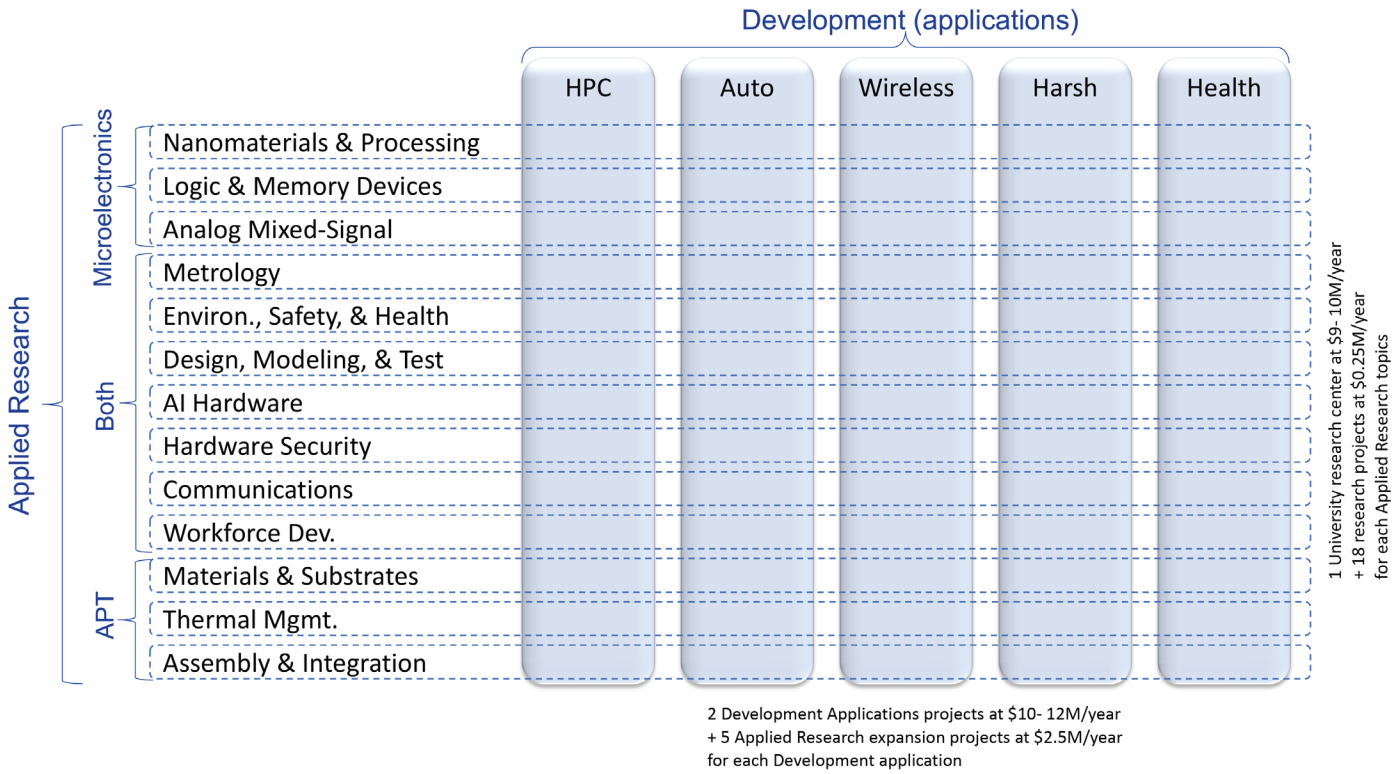


Figure 6. Illustration of how the Applied Research, consisting of Microelectronics and APT fit together with Development (applications) in the MMUSAI.

Basic Research Through DOE, NIST Labs, NSF

This generally exists, but CHIPS funding will restore the discovery of microelectronics-related technology and expand it in future-relevant ways. This will continue to be run by NIST and DOE Labs but is included here for illustrative purposes to show how this fits with MMUSAI. In addition, these groups should participate in collaborate discussions.

- Purpose: Expand knowledge of natural laws and fundamental science
- Topics: Technology related to microelectronics discovery, materials, processing, metrology, quantum computing, high-speed communications
- Topic sourcing: Original ideas and concepts from fundamental principles and natural laws

- Funding source: Congress providing ~$1-2B additional funds to DOE Office of Science and NIST Labs
- IP Rights: Non-exclusive, royalty-free (NERF) to MMUSAI members

Applied Research: NIST-SRC MMUSAI

- Purpose: uses basic science and scientific theory to identify practical solutions
- Topics: Three existing GRC technology programs related to microelectronics, six shared programs, and three APT programs.
    - Microelectronics: Nano materials and manufacturing processing; Logic and Memory Devices; Analog Mixed-Signal
    - Shared: Metrology; Environmental Safety and Health; Design, Modeling, and Test; AI Hardware; Hardware Security; Communications
    - APT: Materials & Substrates; Thermal Management; Assembly & Integration
    - APT/Shared = 60 +/- 5%, Microelectronics/Shared = 40 +/- 5%.
    - Can add/ remove/ merged/ split/ rename with majority ETAB vote
- Topic sourcing: Expansion of discoveries made in Basic Research
- Funding source: $150M by USG/ NIST, $50M cost-share
    - Industry members can be part of some or all technology programs (just like SRC's GRC)
    - Government can distribute their funds across the 12 fields, but must >/= industry contribution in each
- IP Rights: NERF to all members
- Project selection: Reviewed and selected by Government Advisory and Technical Advisory Board(s)
- Annual Budget
    - $110M: 12 university research centers each get $9-10M/year, includes a 10% budget for capex/facilities/ capabilities upgrades
    - $60M: 220 projects at $225K/yr./project (avg.) in each of the 12 technical topics; ~18 projects/topic (~6-8 new projects selected each year)
    - $20M: meetings, collaboration tools, including secure web portal, operational budget
    - $10M: reserved for ad-hoc research projects that accelerate program results

Development: NIST-SRC MMUSAI

- Purpose: Use Applied Research learnings and develop them for applications
- Topics: HPC, Automotive, Wireless, Harsh Environments, Healthcare
- Topic Sourcing: Applied Research and needs defined by industry
- Annual Budget: $200M by USG NIST, $100M cost share
    - $115M: Application development projects with industry + university teams, each of the 5 Development/ Applications topics gets 2 projects at $10-12M/year/project
    - $62.5M: Continuation and 10X expansion of 25 (10%) of the Applied Research projects. Must be with industry-led team which has academic participation
    - $60M: User facilities and piloting capabilities that don't currently exist
    - $30M: Operations, showcase facility (not prototyping for demonstrating capabilities to partners)
    - $30M: Entrepreneurship funds: start-ups and Fellowship funds (think of a distributed instead of centralized Cyclotron Road model, where post-docs work at their universities instead of SF & Boston)
    - $2.5M: Trade and standards
- Performer:

    a. Industry- University teams

    b. University, Nat Lab, incubator services
- Project Selection:

    a. GRC TAB

    b. Government council
- IP Rights: Payers get rights

Demo and Scale Through Industry Incentives

This generally already exists in industry, but incentives from USG for a NSTC and a NAPP would help spur this to the next level and allow for build-out of this, particularly in APT, here in the US. This is essential for national security but is outside of the scope of SRC operation. It is included only to show how it fits with the ideas being proposed.

- Purpose: Provide capital to move towards profitable manufacturing. Generally looking for offtake agreement/ contingent PO. This will be split between NSTC and NAPP
- Technology areas: GRC and beyond

- Annual Budget: $1B by USG, $1B cost share
- USG funds will be matched 1:1 by industry performer to demonstrate and test microelectronics technology
- Mechanisms: could be risk-backed loans, tax incentive, non-federal matching funds
- Performer: small, medium, and large industry members
- Project Selection: USG fund manager
- Project size: $25-100M
- IP Rights: Exclusive to performer, USG gets march-in rights
- Administration: Mitre, Intel, IBM, RTI, etc.

Expected Impact and Measurable Results

Short-term: papers, patents, projects, students/workforce training numbers will be used as a proxy of success. However, these are only an early indicator of the results that matter, not the results themselves.

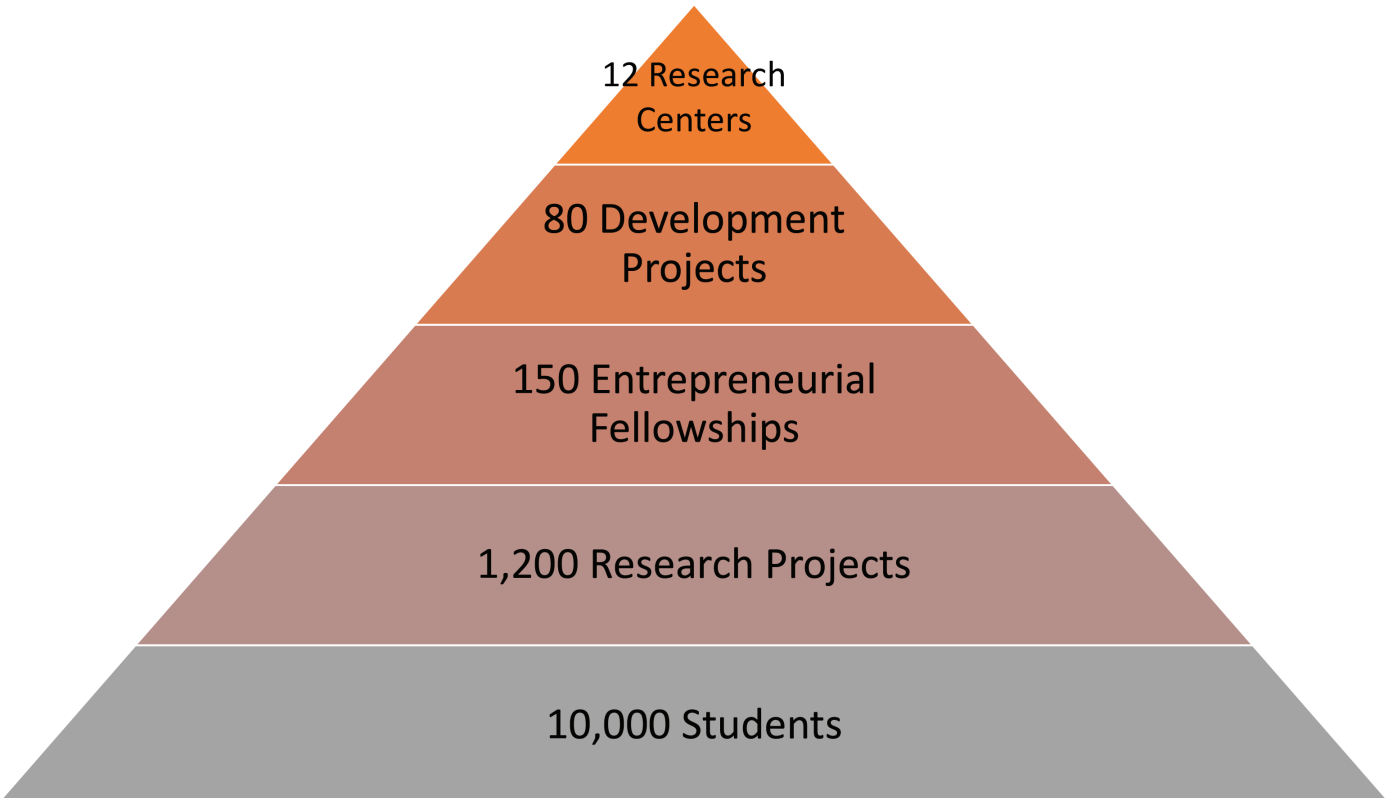


Figure 7. Illustration of the scale needed to initiate the infrastructure that will be built

Long-term: A self-sustained and robust innovation pipeline from ideation through manufacturing to strengthen America's economy and ensure national security. Ambitious metrics include:

- % leading technology manufactured on-shore: grow from 0% to 20%
- Number of jobs in the microelectronics industry: increase by 25%
- Number of critical links in the supply chain remaining off-shore: reduce to zero

Why SRC Should Lead

- Low risk: 40-year history of working with US companies and government across many programs
- Often sited as the go-to organization for Industry- Government-Academia collaboration
- Non-profit, neutral 3rd party with nothing to gain and no ulterior motives or outside influences

- Bring industry for an effective transition to market
- Develop the tech that's shaped the industry for 40 years
- Consistently builds communities where they are needed

- Membership contracts active with 21 industry members, research contracts active with 100 US universities
- Existing processes for managing research and partnering with government
- In-house Technical Program Managers, Contracting, Program Management, Billing, User portal, Legal etc.

Call to Action

Now is the time for SRC to design a large-scale MMUSAI which can solve the problems outlined and capitalize on opportunities. Upon completion, review, and revision of the design, SRC would execute the creation and implementation of this new domestic capability.

The design would include an operational model, budget, timeline, and technology selection. It would also include a tiered membership model and specific goals with deliverables.

Start implementing solutions now by emailing David.henshall@src.org and saying "let's go!"