PIONEERS IN
COLLABORATIVE RESEARCH*

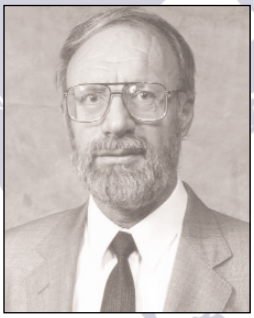
2001

Annual Report

Semiconductor Research Corporation*

The 2001 SRC Annual Report, including financial results, is available online at: www.src.org/member/about/arch/annual01.pdf

Special Dedication



The 2001 SRC Annual Report is dedicated to the memory of Peter Verhofstadt, Chief Scientist of the SRC and Co-Executive Director of MARCO, an SRC subsidiary that manages the Focus Center Research Program.

Peter died on May 10, 2001, after a long and courageous battle with cancer. He received many honors during his career including election as Fellow of the IEEE late in 2000. For the ten years Peter was at SRC he was an energetic and visionary force. He made many outstanding contributions to the industry and all who knew him respected his integrity and valued his friendship.

MEMBERS

Advanced Micro Devices, Inc.
Agere Systems (formerly Lucent)
Chartered Semiconductor Manufacturing (2002)
Conexant Systems, Inc.
Eastman Kodak Company
IBM Corp.
Intel Corp.
LSI Logic Corp.
Motorola, Inc.
National Semiconductor Corp.
Texas Instruments, Inc.
United Microelectronics Corp.

SCIENCE AREA MEMBERS

Axcelis Technologies
Cadence Design Systems, Inc.
Mentor Graphics Corp.
Novellus Systems, Inc.
Shipley Company
Synopsys, Inc.
Ultratech Stepper, Inc.

ADJUNCT MEMBERS

Compaq Computer Corp.
Hewlett-Packard Company (Agilent Technologies)

ASSOCIATE MEMBER

The MITRE Corp.

AFFILIATE MEMBERS

Coventor, Inc.
Integrated Systems Engineering, Inc.
Mission Research Corp.
Numerical Technologies, Inc.
PDF Solutions, Inc.
SILVACO International
Tessera Technologies, Inc.
Testchip Technologies, Inc.
Torrex Equipment Corp.
Ziptronix, Inc.

US GOVERNMENT PARTICIPANTS

DARPA
National Institute of Standards and Technology
National Science Foundation

STRATEGIC SEMICONDUCTOR INDUSTRY PARTNERS

International SEMATECH
Semiconductor Industry Association

2001 Table of Contents

Vision

Semiconductor Research Corporation* (SRC) will provide competitive advantage to its members as the world's premier research management consortium in delivering relevant research results and relevantly educated technical talent.

Mission

SRC's mission is to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the ITRS, focusing on universities
- Relevantly educated university graduates
- Timely transfer of research results
- Strengthened university semiconductor technology capability through partnerships with members
- Collaboration to enhance commercialization and leveraged research.

Message from the President

The 2001 Executive Summary of the *International Technology Roadmap for Semiconductors* (ITRS '01) provides a global consensus view by industry technologists that identifies the R&D needs and potential solutions to maintain the cadence of Moore's Law over a fifteen-year horizon. Most striking in the latest documents are the number and temporal closeness of technology barriers, called "Red Brick Walls," that indicate the areas where there are no known manufacturable solutions to continue the scaling trends.

SRC commissioned an independent study to provide quantitative analysis of the relation between ITRS '01 research needs and resources. It does not appear that the level of research funding directed toward removing technological barriers is adequate. For any single geographic region, e.g., the United States, Europe, or Japan, the estimated gap between resources and needs was approximately $400M per year. This is a significant annual amount but close examination seems to indicate the actual funding shortfall is larger. Much of the research funded in the three regions is redundant, and many of the results are not accessible across regions. This factor serves to reduce the annual effective regional research and thus increases the annual research funding gap. Using estimates of redundancy and accessibility factors, the overall annual research gap result for each region is $750 - $800M.

What is the significance of this result to SRC? It is estimated that 49% - 60% of the needed research is appropriate for a university environment, so SRC should be concerned with how to best address the issue. SRC needs additional revenue in order to better address the research-funding gap.

Moreover, better global research strategic planning, especially between other global research consortia, can make current and increased funding more efficient by providing an opportunity to identify and address redundancy issues as well as to improve the accessibility of research results to common members of cooperating consortia.

Additional SRC revenue is best achieved by increasing the membership base and also by leveraging existing funding through enhanced collaborative efforts. In order to address these opportunities, SRC has developed a new business model, primarily directed at increasing the membership base to address the large research gap, but also to provide mechanisms to enhance cooperation between SRC and research consortia in other regions.

Key elements of the new model provide for including SRC's existing Research Customization Program (RCP) provisions, which enable 20% of a member's fees to be invested in research tasks of interest to the member, together with a new 20% regional investment provision that enables a member's investment in a region of specific interest to the member. A third key element is the possibility of negotiated member discounts. This element requires cooperation/collaboration between SRC and a global research consortium in the region of interest. For instance, if SRC could interest a research consortium in "Region A" to work with us in placing SRC research funds (could include regional and non-regional) or joint consortia funds in "Region A" universities, then the members of "Region A's" consortium could be eligible for a discounted membership in SRC and the members of SRC would be eligible for discounted membership in "Region A's" consortium. Results would be available to the members who are jointly engaged in sponsoring the research, thus broadening the accessibility or results and also providing an opportunity to improve strategic planning of research funding between the cooperating consortia. This also provides a mechanism to control unwanted redundancy.

Our 2001 Board of Directors, under the guidance and leadership of its Chairman, Richard Schinella of LSI Logic, Inc., has worked closely with us again this year to enable SRC to better meet the challenges it faces in these dynamic times. We are indebted to them for their support.

SRC is committed to providing competitive advantage to its members as the world's premier university research management consortium. In order to do that, SRC must be vigilant in sensing coming changes and agile in best exploiting the opportunities that change provides.

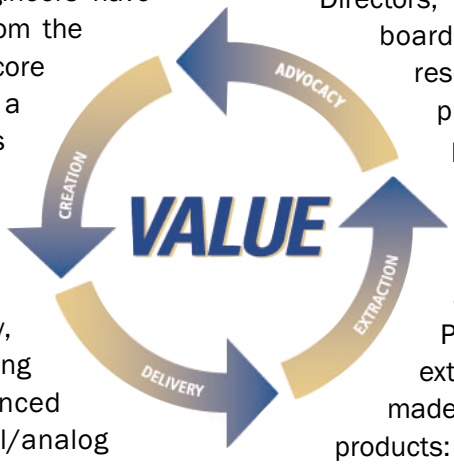
Company Profile

Pioneers in collaborative research®

SRC was launched in 1982 as a non-profit, research consortium to manage long-term, pre-competitive research in semiconductor technology at U.S. universities and to develop the relevantly educated talent to meet the needs of the industry. Over the past 19 years the industry has invested more than $550 million through the SRC, and well over 3000 scientists and engineers have received advanced degrees from the supported programs. The SRC core directed research program has a portfolio of over 300 projects currently targeted at the full spectrum of semiconductor technologies, including circuit and system design, design tools, test and testability, materials processes, packaging and interconnect, advanced patterning; mixed signal/analog technologies, metrology, environmental, safety, and health, advanced device, and modeling and simulation. The SRC subsidiary, MARCO, has four Focus Center Research Centers that are described in the MARCO annual report.

SRC continued to enhance student programs in its core program to ensure development of the highest quality talent for our member companies. In addition, the SRC Education Alliance, described on page 11, addresses the need for developing undergraduate talent relevant to the industry.

Because the semiconductor industry and its International Technology Roadmap for Semiconductors have become global, SRC now has members and university research programs in countries around the world. In order to enable the most effective approach for delivering our value to our member companies, research results and publications are posted on the secure web site for member access. In 2001 a record number of publications and deliverable results were placed on the site along with the patents and software to which the members have royalty-free access. Also in 2001, the site was used for real-time collaboration as well as threaded discussions via newly added features.



Through the combined efforts of the Board of Directors, the various technical advisory boards, and the SRC staff, the research strategy and operation plans are continually refined to produce value satisfying the members as evidenced by the annual member satisfaction survey. The survey addresses all four dimensions of the Value Proposition—creation, delivery, extraction, and advocacy—that are made available via the SRC's primary products: Research Results, Relevantly Educated Talent, Integrated University Research Capability, and Networking. We have continued to hone the processes and tools associated with the delivery of SRC value to the member companies. Also, we have continued to refine the mechanisms and support that are provided to facilitate the extraction of maximum value in the most cost-effective manner for our member companies, as evidenced by the increased use of electronic meetings utilizing the SRC web site. Finally, we work with the representatives of our member companies on the Board of Directors and the various advisory boards to revitalize continuously our products, programs, processes and systems to enhance value for our members.

Company Profile

Year 2001 was a particularly difficult year for the industry and for SRC. The marketplace underwent significant changes that have in turn changed the complexion of the industry, the research needs, and the research budgets. As a result, preparation for Year 2002 presented even greater challenges to maintain critical research programs and to maintain the SRC reputation of being one of the preferred sponsors of university research. Several examples of the dynamic nature of our business and the value that the community of our consortium has brought forth in the year 2001 are presented in various sections of this report. This abbreviated report can only describe some of the key accomplishments, major initiatives, and important events of the year 2001 that demonstrate the value, strength, and agility of the consortium, for example:

- SRC conducted the ETAB Summer Study, a biennial strategic event. At the 2001 Summer Study the SRC Executive Technical Advisory Board, in collaboration with academia, government agencies and International SEMATECH, developed long term directions for the SRC research portfolio. These groups defined new areas that would expand the scope of our research program in four domains: Optoelectronics, Embedded Software, Ultra-Low-Power (<10microwatt) Systems, and Innovative Patterning.
- The SRC Board of Directors approved a new business model, outlined in the Message from the President, that comprehends the global, diverse nature of the consortium. **(page 2)**
- NSF and SRC developed a partnership in 2001 to fund a major program in an array of mixed signal technologies. **(page 5)**
- The SRC Compact Modeling program made several significant advances including the development of a closed-form surface potential model that substantially increases computational efficiency. **(page 6)**
- Professor Jason Cong received the Technical Excellence award for his work in "Interconnection Estimation, Planning, and Synthesis for Deep Submicron Designs". **(page 9)**
- An International Graduate Fellowship Program was initiated with an international Fellow named at the University of California at Berkeley. **(page 10)**
- Nine SRC-sponsored U.S. and foreign patents were issued, bringing the total portfolio of SRC-licensed patents to 178, all of which can now be queried by members on the SRC web site. **(page 13)**

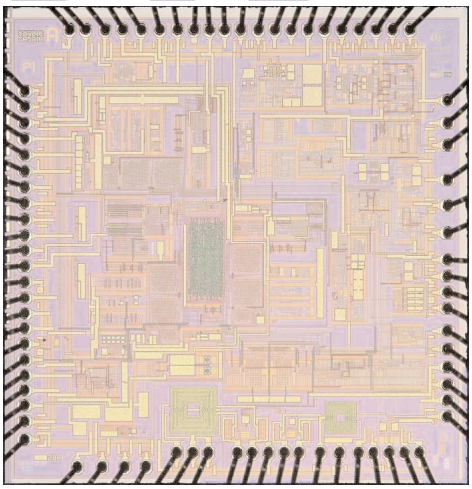
In addition, there were many other noteworthy accomplishments not described in this abbreviated report, such as:

- In 2001 the member companies assigned a record number of Industrial Liaisons to work with the researchers on a record number of tasks, a strong indicator of the ongoing efforts to derive value from the technology and to mentor the students toward a rewarding career in the industry.
- In 2001, SRC not only launched a completely new database-backed web site, it also established an information architecture and technology infrastructure that enabled the rollout of the MARCO/FCRP Web site and the SRC Education Alliance Web site utilizing a common database, security and technology base.
- In 2001, in its first foray into electronic collaboration, SRC launched "The Hub" as a web-based collaboration environment accessible to registered users from the SRC, MARCO/FCRP and Education Alliance Web sites for purposes of electronic discussion and document sharing.

Research Contributions

Mixed Signal Initiatives

The technology node schedule has again been pulled forward by the 2001 version of the International Technology Roadmap for Semiconductors (ITRS '01) and at the same time, ITRS '01 reflects emerging requirements for important new applications, such as mixed signal technologies and novel device/interconnect concepts. SRC responded to this challenge in 2001 by continuing to push its technology research horizons, while addressing a broader venue of semiconductor technology applications. For example, NSF and SRC developed a partnership in 2001 to fund a major program in an array of mixed signal technologies ranging from devices and interconnect through design and test to CAD and packaging for mixed signal applications. In addition, SRC became a member of the NSF CDADIC Industry/University cooperative research consortium on analog integrated circuit design to increase the generation of new design ideas and graduates in this key area. An important emphasis in design, driven by increasing IC complexity and performance, is the area of low power and low voltage design. SRC has created strong research programs that are providing new concepts and design methods for low power/low voltage systems. Examples include a 2.4 gigahertz, 91 milliwatt frequency synthesizer operating at 1.8 volts and a 10 gigabit per second per pin chip-to-chip interface using incremental sampling.



A highly integrated RF Mixed Signal I.C. from Conexant using their .35um Silicon Germanium BiCMOS Process

CMOS Devices & Beyond

Work to extend the life of bulk planar CMOS technology continued unabated in 2001 and several salient results have been obtained. Working with our colleagues at International SEMATECH, (ISMT) we have developed promising candidates for the MOSFET gate stack material replacement for the SiO_2 gate dielectric and the gate electrode together with associated processes for the gate stack. We have developed two fundamental approaches to guide the selection of new gate dielectrics: one approach is based on the localized molecular orbital description of transition metal non-crystalline silicate and aluminate alloys and the second uses the Tight Binding (TB) approximation and density functional theory (DFT) of solid state physics. The

Research Contributions

SRC/ISMT work has led to identification of the promising Hf-based (HfO_2 and HfO_2-SiO_2) candidates for the new high-K gate dielectric. Looking beyond planar CMOS, we are exploring new non-classical MOSFET structures that have the potential to overcome the major limitations of conventional bulk CMOS structures. Indeed, several of the double-gate structures that we are examining appear to promise extension of CMOS to the end of the time horizon of the current 2001 ITRS '01 (22 nanometer node with a physical gate length of 9 nanometers). Although it appears that CMOS technology can ultimately be extended to provide manufacturable MOSFETs in the sub 10 nanometer channel length regime, it is probable that the MOSFET will ultimately need to be supplemented with other novel information processing devices. SRC has surveyed the landscape of potential devices that have been proposed to date, including novel ultimate CMOS devices, and we have launched a few exploratory projects on some of the more promising ideas.

Device and Compact Models

The design and application of devices and systems as scaling continues requires the development of predictive models that accurately represent device and circuit performance. In 2001, SRC researchers demonstrated the applicability of a Non-Equilibrium Green's Function method to performing full quantum simulations of 10 nanometer MOSFETs and other novel nano-scale devices. This new method will help to support the design choices that need to be made in device structure and material composition. Compact models must be available for use by circuit designers to enable them to rapidly utilize aggressively scaled devices. The SRC Compact Modeling program has made several significant advances in 2001 including the development of a closed-form surface potential model that substantially increases computational efficiency. Compact models, e.g., BSIM, are the *lingua franca* of inter-company technical communication and are an important element of the SRC research program. As such, these models are increasingly being utilized to provide a predictive capability to explore the performance of the advanced technology nodes in addition to being descriptive of the current technology nodes.

Design Systems

The ability to efficiently design high performance chips containing many millions of transistors is another challenge that is being addressed by SRC. For example, we have developed a new placement method that is ten times faster than previous methods and we have developed physical design methodologies to predict interconnect power consumption that can lead to a fifty percent power reduction relative to conventional techniques. We have also continued our research in formal verification tools for integrated circuits and are gratified that many of our members are deriving substantial benefit from this work. To address the urgent need for economical test methods for Systems on a Chip which incorporate a mix of analog, digital, radio frequency, and microelectromechanical elements, we have recently shifted the focus of our test research toward built-in test of mixed signal systems. Spectral methods, time-domain analysis of power supply waveforms, and other surrogate methods are being developed, as well as methods which utilize processing capabilities of the on-chip circuitry to analyze other parts of the chip.

On-Chip Interconnect

SRC research in on-chip interconnect technology is focused on extending the use of metal-dielectric systems as far as possible on the ITRS 2001 node sequence. New processes and materials are being explored

for inter-level dielectrics and for diffusion barriers between the copper and dielectric layers. For example, we have shown that it may be possible to eliminate the need for CVD or PVD seed layers prior to deposition of copper on a metal nitride barrier film. We have developed a 2-D feature scale model for Cu/SiO2 damascene wafers. We have also demonstrated a possible "zero thickness" barrier that could revolutionize the copper dual damascene process. The time-delay situation for long distance metal/dielectric interconnect systems undoubtedly will worsen as we advance through the ITRS '01 technology nodes; however new architectures and design methodologies may forestall the transition from metal/dielectric to other technologies for several ITRS '01 nodes. For example, current injection signaling and proper signal design may decrease interconnect power consumption and cross-talk and also reduce the number of repeaters required, relative to voltage signaling.

Packaging

SRC research in packaging is addressing advanced packaging opportunities to effectively transfer the advances made in chip performance to the electronic system. Packaging research is also exploiting new package/chip co-design paradigms to address roadblocks to on-chip performance identified in the ITRS '01. Recent advances have provided methodologies to design very high frequency, high performance packages for mixed signal and high performance processor applications. New research has also provided unique IC clock distribution methodologies that employ the package lid as a high performance signal coupling medium between circuit blocks on a single chip. SRC programs are rapidly identifying key indicators of adhesion failure in layered dielectrics - a critical issue for modeling failures in both packaging materials and on-chip low k dielectrics.

Patterning

There is optimism that one or more of the Next Generation Lithography (NGL) tools under development will be able to sustain the ITRS '01 cadence for the most advanced technology generations. SRC research is studying low-cost, high performance options that might initially complement NGL tools and ultimately lead to post-NGL approaches. To that end, SRC research is underway to identify new patterning technologies, e.g., maskless patterning and self-assembly. This work is buttressed by excellent research on metrology to support mask-making and NGL technologies as well as nanostructure measurements. We have continued our tradition of leading-edge contributions to resist technology with programs in resist modeling and synthesis, image formation, and modeling of pattern transfer.

Process Models

SRC conducts research to develop models for a wide variety of semiconductor processes. Our fundamental research in plasma modeling has focused on the development of linkages between equipment-level models and feature scale models for the actual structures produced on the wafer. In ion implantation, a universal species ion implant model has been proposed, implemented, tested, and verified based on the theory of electronic stopping power. Experimental data has validated the model accuracy from boron to tungston. Also, models for boron, boron phosphorus, phosphorus, and arsenic ion implant have been developed and verified to be accurate over the entire implantation depth profile and are applicable over a wide range of implantation variables (e.g., energy, dose, tilt angle, rotation angle, etc.) and physical conditions (e.g., topographically varying surfaces, multiple layers, mask edge effects, and screening oxides). As another example of process research, we are developing an understanding of the fundamental

Research Contributions

mechanisms of the activation and deactivation processes for dopants to provide insight into optimizing and controlling activation.

Environmental, Safety, & Health

Our research philosophy is to anticipate the evolution of tools, materials, and processes and to concurrently embed Environmental, Safety, and Health considerations in the development of new high performance materials and processing technologies. The primary mandate for this aspect of SRC research is held by the NSF/SRC Engineering Research Center (ERC) on Environmentally Benign Semiconductor Manufacturing. This ERC has provided significant findings that promise to provide substantial emission reduction through alternate chemistries for plasma processing. Another ERC strategy is to achieve process simplification and to minimize the generation of by-products from semiconductor processes; e.g., via techniques such as the supercritical CO_2 develop to replace wet resist removal processes. This ERC has also focused on methods that reduce raw-material consumption and has achieved notable success in the area of reduction in water use requirements for factory operations.

Factory Operations

The effective operation of a semiconductor factory is essential in view of the costs of operation and the capital investment that exceeds one billion dollars today. SRC and ISMT are collaborating to support an international university research program directed toward developing factory operating procedures to increase the efficiency of capital utilization under a representative mix of product needs and equipment outage conditions. Projects that are contributing to member factory operations include: the development of software tools for optimum preventative maintenance scheduling; optimum demand aggregation to minimize inventory cost and support capacity planning; and, efficient facility simulation techniques that are 'resource driven' rather than 'job driven.'

Cross-disciplinary Research

The technical challenges faced by the semiconductor industry do not always submit to compartmentalization by technical discipline, but instead require the best efforts of specialists from many disciplines. During 2001, SRC has increased emphasis on cross-disciplinary research to address modeling and simulation and mixed signal systems as well as other technical areas. We expect that the cross thrust initiatives and reach-out research on alternate solutions to the ITRS '01 challenges will be a growing part of the future SRC portfolio and we are already seeing benefits from our endeavors. For example, we have developed tools that guide design by directly relating the physical design of the chip to the quality of feature production that can be achieved by lithographic tools. Also, the reach-out research on device, materials and processing, may lead to radical solutions to many of the grand challenges facing CMOS scaling.

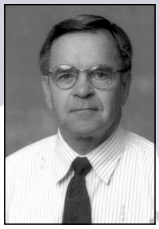
Scope

The SRC research program in 2001 encompassed 350 research tasks at 75 universities and involved 250 faculty researchers and 1200 students. SRC continued to be recognized by more than 90 percent of the faculty participants as a research sponsor of choice.

Award Recipients

Aristotle Award

The 2001 Aristotle Awards were made to Professor Rob Rutenbar, Carnegie Mellon University and to Professor Gerald Neudeck, Purdue University. The Aristotle Award recognizes SRC-supported faculty whose deep commitment to the educational experience of SRC students has had a profound and continuing impact on their professional performance and consequently a significant impact for members over a long period of time.



NEUDECK

RUTENBAR

Technical Excellence Award

Professor Jason Cong, of UCLA, was the recipient of the Technical Excellence Award for his work in "Interconnect Estimation, Planning and Synthesis for Deep Submicron Designs." This award is given annually to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research, who are ground breakers and leaders in their fields, and who are regarded as model collaborators with their colleagues in the SRC member community.

CONG

Mahboob Khan Award

The Mahboob Khan Outstanding Mentor Award, named in memory of a long-time SRC Industrial Liaison program advocate from Advanced Micro Devices, is presented each year to those individuals who have made significant contributions in their roles as Industrial Liaisons. Recipients represent "ideal mentors" whose commitment more than enhances the SRC research program. The 2001 award recipients were:

Charles J. Alpert of IBM Corp, who has worked with Dr. Sachin Sapatnekar and his students at the University of Minnesota effectively for several years. The work resulted in several coauthored papers, one being selected for the Best Paper Award at DAC 2001. He has encouraged the students to develop solutions to real industry issues, and he contributed to the incorporation of these results into IBM's design methodology.

Dejan Jovanovic of Motorola Inc., has been especially proactive in forging a strong collaborative program that is benefitting Purdue University, Motorola and SRC. His work with SRC student Ramesh Venugopal has resulted in the co-development of improved numerical methods and physical models. The work was presented as a joint publication at last year's IEDM.

Robert Kurshan of Lucent Technologies (Bell Labs), is a long time participant in mentoring activities at Carnegie Mellon University and, more recently, the University of Texas/ Austin and the University of Utah. Bob's contributions in the areas of formal verification and model checking have become the industry standard. He has made special effort to meet with new investigators and provide practical examples to guide their research program to success.

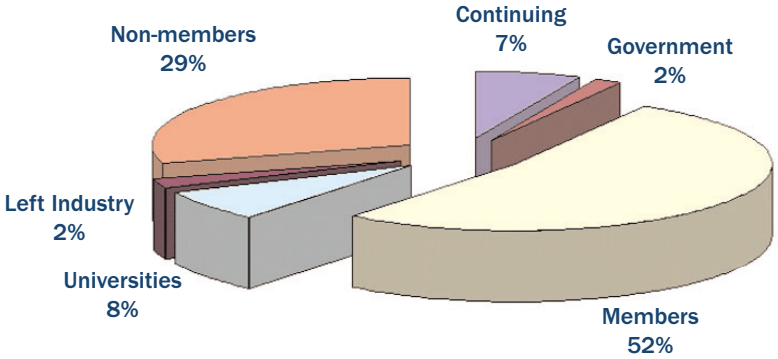
Student Programs

SRC hosted the first TechConnect in April 2001 at Stanford University. The event provided an opportunity for SRC-supported students to interact with industry representatives, and included a panel discussion and presentations by several former SRC students.

Over 1,200 students participated in SRC-funded research in 2001. Of the graduates, about 70% went to work for SRC member organizations or are undergraduates continuing to graduate school, further strengthening the links within the SRC community. Other 2001 accomplishments included:

- Nine new core Fellowships, 7 new Company-Named Fellowships, and 1 new Research Fellowship were awarded through the Graduate Fellowship Program to bring the number fellowships at the beginning of the 2001 fall term to 54.
- The International Graduate Fellowship Program was piloted with an International Fellow named at the University of California at Berkeley. This was a first step toward creating student programs for the benefit of SRC's international members.
- The Master's Scholarship Program was expanded to include 4 Company-Named Scholarships, 2 IBM/SRC Scholarships and 2 National Semiconductor/SRC Scholarships. A total of 14 Scholarships were in place at the beginning of the 2001 fall term. More information on the Fellowship and Scholarship Programs can be found on the SRC Web site at www.src.org/member/students/fellowships.asp.
- Over 400 student resumes were published on the SRC Web site and a directory of non-SRC students at SRC-funded universities was created on the Web.
- The annual Student Programs Brochure was published to provide student information for members and prospective Fellows and Scholars
- The Undergraduate Engineering Programs were very successfully launched and the Simon Karecki Endowment established under the SRCEA (see p. 11).

2001 SRC STUDENT HIRING STATISTICS



Sixty-nine percent of students completing degrees under SRC-funded research in 2001 joined member organizations or are continuing to higher degrees.

SRC Education Alliance

UEP Sponsoring Companies

- Advanced Micro Devices, Inc.
- Agere Systems
- Agilent Technologies
- Analog Devices, Inc.
- Conexant Systems, Inc.
- Cypress Semiconductor Corp.
- IBM Corp.
- Intel Corp.
- Intersil Corp.
- LSI Logic Corp.
- MICRON Technology, Inc.
- Motorola, Inc.,
- National Semiconductor Corp.
- Texas Instruments Inc.,
- Xilinx, Inc.

The SRC Education Alliance is a wholly-owned subsidiary of the Semiconductor Research Corporation. The SRCEA is a non-profit (501 (c) 3) charitable foundation with strong ties to the SRC research and student programs.The Undergraduate Engineering Programs and the Simon Karecki Endowment are managed under the SRCEA.

The Undergraduate Engineering Programs were successfully launched in July 2000 with the first year completing in June 2001. These programs were funded by SIA Board member companies.

Undergraduate Engineering Programs Year One: Assessment and Recommendations was published in October 2001 and is on the SRCEA Web site at http://srcea.src.org/programs/default.asp.

Ninty-one individual students at 37 universities participated in the Undergraduate Research Assistants Program. The program has attracted a relatively high percentage of women (37%) although no emphasis has been placed on under-represented populations. Of the first group of eleven graduates, two have joined sponsoring companies, six are continuing to graduate study, one has joined a telecommunications/networking company, and one has joined the US Army Corps of Engineers. Feedback from participating faculty and students has been entirely positive, noting benefits to research programs, faculty, undergraduate and graduate students, and the semiconductor industry.

Funding for the MOSIS Educational Program has provided the stability necessary not only to stem the downward spiral that ensued with the end of government funding, but also to create a significant upturn in 2001. A survey of participating faculty indicates that the program will not only reach its former level, but has considerable potential for growth if stable funding is maintained.

The Simon Karecki Endowment was established in Simon's memory and to fund annually, a fellowship and/or a cash prize through the SRC/NSF Center for Research in Environmentally Benign Semiconductor Manufacturing. The first award will be made at the Center review in 2002. More information is available at http://srcea.src.org/programs/karecki/default.asp.

The SRCEA was honored with the President's Medallion from the University of Central Florida for partnering with the Electrical Engineering and Computer Science Program. The Undergraduate Research Assistants Program has supported four undergraduate students at UCF.

Focus Center Research Program

SPONSORS:

Semiconductor Industry Association (SIA):
- Advanced Micro Devices, Inc.
- Agere Systems
- Agilent Technologies
- Analog Devices, Inc.
- Conexant Systems, Inc
- Cypress Semiconductor
- IBM Corporation
- Intel Corporation
- LSI Logic Corporation
- MICRON Technology, Inc.
- Motorola, Incorporated
- National Semiconductor
- Texas Instruments
- Xilinx, Inc.

Semiconductor Industry Suppliers:
- Air Products & Chemicals, Inc.
- Applied Materials, Inc.
- KLA-Tencor Corporation
- Novellus Systems, Inc.
- SCP Global Technologies
- SpeedFam-IPEC
- Teradyne, Inc.

Department of Defense:
- Deputy Undersecretary of Defense for Science & Technology
- Defense Advanced Research Projects Agency (DARPA)

DESIGN AND TEST

The Design and Test Focus Center or Gigascale Silicon Research Center (GSRC) addresses concepts such as component/communication-based design, constructive fabrics, fully programmable systems, calibration of achievable design, validation, power and energy. The University of California at Berkeley leads a team of researchers from fourteen U.S. universities. The Director of the center is **Professor Richard Newton.**

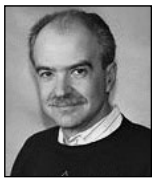
UC/BERKELEY
- Carnegie Mellon University
- Mass. Institute of Technology
- Pennsylvania State
- Princeton University
- Purdue University
- Stanford University
- UCLA
- UC/San Diego
- UC/Santa Barbara
- UC/Santa Cruz
- University of Michigan
- Univ. of Texas / Austin
- University of Wisconsin

INTERCONNECT

The Interconnect Focus Center is headquartered at the Georgia Institute of Technology. **Professor James Meindl** is the center's director. The center's team of researchers from six U.S. universities is pursuing six major tasks: system architecture and circuit innovation that "keep the wires short", physical design tools for 3D integration, novel RF and optical communications mechanisms, integrated input/output interconnects, materials and processing, and an atomistic approach to predictive modeling and metrology.

GEORGIA TECH
- Massachusetts Institute of Technology
- Rennselaer Polytechnic Institute
- Stanford University
- Univ. of Albany
- UCLA

MATERIALS, STRUCTURES & DEVICES



Professor Dimitri Antoniadis of the Massachusetts Institute of Technology is the Director of the Materials, Structures and Devices Focus Center. He leads a team of ten U.S. universities. This center will research sub-10-nanometer silicon-based FETS, silicon-based quantum-effect devices, molecular and organic semiconductor electronics, carbon nanotube-based electronics and device modeling & simulation.

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- Cornell University
- Princeton University
- Purdue University
- Stanford University
- University of Albany
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- University of Virginia

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The Circuits, Systems and Software Focus Center (C2S2) is a multi-university team of ten U.S. universities led by Carnegie Mellon University. **Professor Rob Rutenbar** is the Director. The center's research will focus on rapid synthesis of analog/mixed signal circuits, explore novel system level technologies and search for software solutions and work-arounds for deep submicron CMOS process limitations.

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- Cornell University
- Massachusetts Institute of Technology
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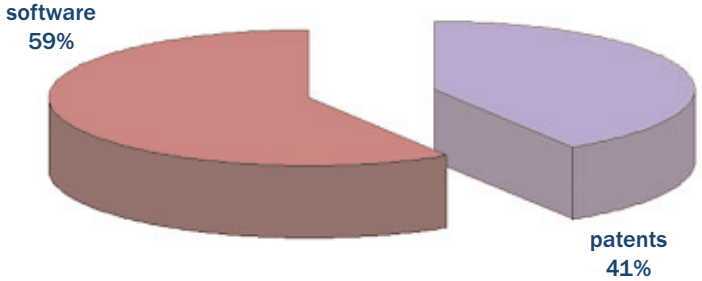

U.S. Patents ISSUED IN 2001

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Current Signatures for IDDQ Testing	Wojciech Maly Anne Gattiker	Apr. 25, 1997 Jan. 16, 2001	6,175,244	Carnegie Mellon University
Method for Diagnosing Bridging Faults in Integrated Circuits	Brian Chess Joel Ferguson Tracy Larrabee David Lavo	Nov. 3, 1997 Mar. 13, 2001	6,202,181	Univ. of California at Santa Cruz
Method for Testing and Diagnosing MOS Transistors	A. Neugroschel Chih-Tang Sah	Oct. 4, 1999 Aug. 14, 2001	6,275,059	Univ. of Florida
Uncooled Infared Focal Plane Imager and Microelectromechanical Infared Detector for Use Therein	Chien-Chang Liu C. Mastrangelo	Oct. 14, 1999 Oct. 9, 2001	6,300,632	Univ. of Michigan
Silicon-on-Insulator Transistors Having Improved Current Characteristics and Reduced Electrostatic Discharge Susceptibility	Chenming Hu Mansun Chan Ping Ko Hsing-Jen Wann	Aug. 4, 2000 Oct. 9, 2001	6,300,649	Univ. of California at Berkeley
Films for Use in Microelectronic Devices and Methods of Producing Same	Jeffry Kelber	July 27, 2000 Oct. 23, 2001	6,306,495	Univ. of North Texas
Floating Gate Transistor Having Buried Strained Silicon Germanium Channel Layer	Sanjay Banerjee David Kencke	Jun. 15, 2000 Nov. 6, 2001	6,313,486	Univ. of Texas at Austin
Vertical Channel Floating Gate Transistor Having Silicon Germanium Channel Layer	Sanjay Banerjee David Kencke	Jun. 15, 2000 Nov. 6, 2001	6,313,487	Univ. of Texas at Austin
High Mobility Heterojunction Transistor and Method	Sanjay Banerjee Q.C. Ouyang Al Tasch	May 9, 2000 Nov. 20, 2001	6,319,799	Univ. of Texas at Austin

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** Dan Casaletto served on the Board through Nov. 7, 2001. Don Harbert took his seat on Nov. 8, 2001.

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