

# Strategic Research for a Dynamic Industry



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SEMATECH  
Semiconductor Industry Association

*This annual report is dedicated  
to James F. Freedman*



*A recap of 1998 would be incomplete without mention of the retirement of James F. Freedman.*

*The following is an excerpt from Larry Sumney's remarks at the retirement event honoring Jim Freedman ... "One of Jim's most valued contributions to the SRC is his leadership for TECHCON. He served as General Chairman for TECHCON '88 in Dallas, TECHCON '90 in San Jose, TECHCON '93 in Atlanta, TECHCON '96 in Phoenix and TECHCON '98 in Las Vegas. The early TECHCONS included faculty presentations and student posters; TECHCON '98 was entirely student presented and included 228 papers and posters. Jim was recognized by his colleagues after TECHCON '96 this way, 'If I had to summarize the best of Jim over all of the TECHCONS, it is that he has always had the ability to lead when needed, delegate ownership and responsibility whenever possible, and then defend and support his staff in all battles great and small.'"*

*TECHCON is very likely Jim's legacy to SRC; it provides a forum for looking very closely, on a regular basis, at the research and the way results are delivered to decide that SRC does make a positive difference.*

## Vision

Semiconductor Research Corporation (SRC) will provide competitive advantage to its members as the world's premier research management consortium in delivering relevant research results and relevantly educated technical talent.

## Mission

SRC's mission is to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the NTRS, focusing on universities
- Relevantly educated university graduates
- Timely transfer of research results
- Strengthened university semiconductor technology capability through partnerships with members
- Collaboration to enhance commercialization and leveraged research

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The annual report of the Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC research program, present the formal financial report and provide information on activities and events of the SRC community for the previous calendar year.

A copy of this report and additional information about SRC are accessible on the World Wide Web at <http://www.src.org>.

# Message from the President & CEO



Larry W. Sumney

Each day, SRC focuses on the future of our dynamic industry. During the past year, SRC's member companies, university researchers and government partners, and our dedicated staff, have positioned themselves to begin the 21st century in an increasingly complex environment.

To align with the industry's continuing evolution, SRC has analyzed and reviewed its core program research structure and combined its seven previous science areas into four:

1. *Computer-Aided Design and Test Sciences (CADTS)*
2. *Integrated Circuits and Systems Sciences (ICSS)*
3. *Materials and Process Sciences (MPS)*
4. *Nanostructure and Integration Sciences (NIS)*

In addition, SRC has created a special Cross-disciplinary Semiconductor Research (CSR) program that encourages initiatives for high-risk research addressing long-term needs of the industry.

## What is Next for Technology?

The industry will progress toward 100 nm technology nodes with little interruption in cadence. 193 nm lithography tools will probably suffice to enable this progress, with increasing efforts to add product value through integration of analog/RF signals with digital signals on a single chip. Industry growth will be spurred by expanding applications and very high-performance/functionality products.

At, or slightly beyond the 100 nm node, the quality of MOSFET transistors will decline, the performance enhancements due to copper interconnect systems will lessen, new lithography technologies will be needed, new metrology technologies will be required, packaging problems will become more challenging and the tension between the need to design at high levels of abstraction for productivity enhancements and the need to utilize more sophisticated (and complex) deep submicron physical device models will be heightened.

*In order to address these issues, we are working with SRC members and our university partners to:*

- Discover new integrable gate dielectrics and new shallow junction technologies to provide high quality MOSFETs below 100 nm
- Invent new low-K interlevel dielectrics to extend the benefits of copper interconnect technologies
- Develop new chip architectures that minimize the need for global connections to extend the price-performance gains for IC technology at the rate provided by industry for three decades
- Support the challenge of defining technologies for future generations of patterning systems
- Advance the state of metrology for critical dimensions, doping distributions, etc., needed for below 100 nm production
- Create new generations of interconnect-aware IC CAD tools and test strategies
- Explore novel self-assembly methods that could offer lower complexity processes for IC fabrication
- Begin to blend IC and molecular technologies to develop self-configuring architectures that lower fabrication costs.

This scenario of possibilities is exciting, and can result from SRC's continued focus on the future. Our commitment will pay off, for our industry, and in solutions to human problems and applications we have yet to imagine.

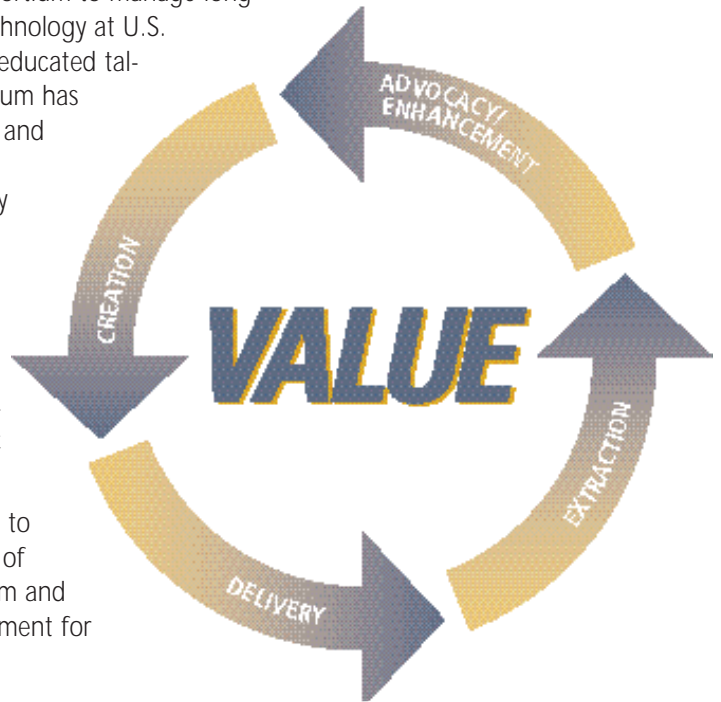
Sincerely,

Larry W. Sumney  
President & CEO

# About SRC

SRC was established in 1982 as a research consortium to manage long-term, pre-competitive research in semiconductor technology at U.S. universities and, in doing so, develop the relevantly educated talent to meet the needs of the industry. This consortium has consistently produced and delivered research results and relevantly educated students over the past 17 years. Obviously, the research and the students are strongly interdependent. SRC directs a set of research programs, over 300 projects, carried out at over fifty leading universities now throughout North America. These programs are funded by the member companies comprising of the full value chain of the semiconductor industry including the infrastructure companies (materials, equipment and tools for use by IC companies) as well as the IC product.

SRC's long, productive existence is a testimonial to the vision and dedicated commitment of thousands of individuals in the entire community of the consortium and has proven to be an excellent and enduring commitment for cooperative research.



## SRC's Value

The members of SRC consortium have identified four products which they consider as critical to providing value to them. These products are:



### Research Results

SRC sponsors university research that is responsive to the critical challenges identified in the National Technology

Roadmap for Semiconductors (NTRS). Technology solutions are key to maintaining the pace of evolution of the technology roadmap necessary for continued health and profitability of the semiconductor industry.

### Relevantly Educated Talent

Graduate students engaged in carrying out SRC-sponsored research represent the highest quality of students. SRC research programs prepare them to be the talented scientists and engineers our members need to ensure success.

### University Infrastructure

Through the sponsorship of universities, SRC has helped to establish an infrastructure of talented faculty which provides resources for the industry to utilize for solving their specific, individual problems.

### Networking

The consortium provides a forum for the industry, university and government experts and managers at a variety of levels to interact with peers. These interactions provide numerous opportunities for benchmarking.

The SRC team must continuously focus on all dimensions of the value. We must help create the value through the products described above, deliver it in the most effective way, facilitate our members to extract it in a most cost-effective manner and enhance it on an ongoing basis. The semiconductor industry is one of the most rapidly changing industries. These changing business conditions change our member companies' needs continuously. We are committed to providing the most value to our

# About SRC

members by anticipating, adapting and responding to their changing needs. In order to keep the consortium strong and dynamic, we work with the representatives of our member companies on the Board of Directors and various advisory boards to continuously revitalize our products, programs, processes and systems. Some examples of the dynamic nature of our business and the value that the community of our consortium have brought about in 1998 are presented in various sections of this report.

*Some of the major initiatives and events during 1998 which demonstrate the value, the vitality and the dynamic nature of our consortium include:*

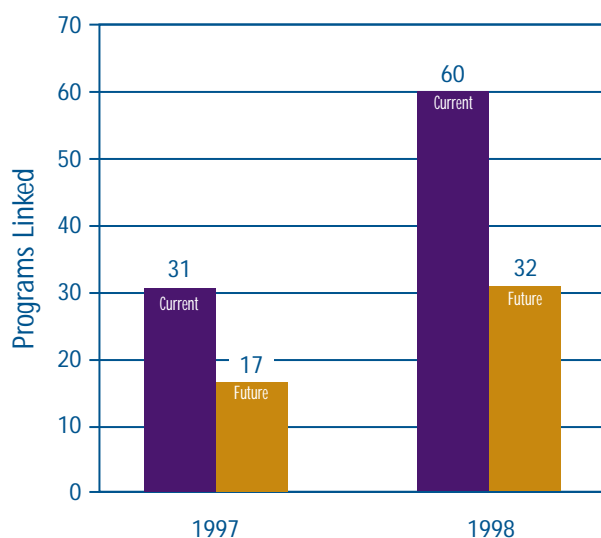
- Initiation of research in Front End Processes (FEP) for technology nodes <100nm by sponsoring an FEP Center in collaboration with our strategic partner, SEMATECH.
- Launching of the two Focus Centers dedicated to very long-term (7-8 yrs) research in the areas of Design and Test and in Interconnect Sciences (Page 17).
- A highly successful and valuable TECHCON, our biannual Technical Conference to showcase the best of both our research dollars and students.
- Restructuring of our Science Areas, based on member input and anticipating their future needs (Page 10).
- Some of our highly coveted awards that recognize the value provided by various constituents of the SRC community, such as the Aristotle Award (Page 13), the Technical Excellence Award (Page 14), and the Industrial Liaison Award (Page 15).

## Stronger Partnership with SEMATECH

In addition to the focus on the intrinsic value from SRC, we have also endeavored to maximize the value for our members from the entire chain of R&D performed in the two sister consortia, SRC (both FCRP managed by MARCO and the core programs of SRC) and SEMATECH. Working with the Executive Technical Advisory Boards and the senior management of these two consortia, we have developed and implemented a model and processes, and coordinated schedules to link Strategic Plans of

these organizations. This allows a more robust research portfolio, which incorporates inputs from SEMATECH (whose primary mission is R&D in manufacturing infrastructure). The linkage also allows, where appropriate, well-planned technology flow from SRC research results to "Technology Hardening" by SEMATECH.

## SRC Programs Linked to SEMATECH Projects



In 1998, SEMATECH and SRC increased by twofold over 1997 the number of programs with high interconsortia relevance. Higher relevance means an increased likelihood that SRC-sponsored university research will be taken up by SEMATECH and commercialized through a supplier partner, resulting in equipment or processes that can be inserted into member company fabs.



*Larry Sumney (SRC), with Mark Melliar-Smith (SEMATECH) at TECHCON '98.*



# Research Contributions

*SRC's research is accomplished through the efforts of world-class university professors and their graduate students supported by industrial liaisons from the member companies and SRC's science area directors. In 1998, research results were very well aligned with the "difficult challenges" as identified in the National Technology Roadmap for Semiconductors. Details of the 1998 research results can be found on the SRC Web site. Below are some of the significant highlights.*

## Design Sciences

**Processor Verification** - An increasingly difficult challenge of microprocessor design is assuring correct operation before product manufacture and shipment. Three investigators working in formal verification made advances in proving processor correctness, and helped raise correctness demonstration to a higher level. Professor J. Strother Moore and his students at UT-Austin developed a formal description of a multi-issue, speculative execution machine and techniques for verifying the difficult exception handling mechanisms. Professor Randy Bryant and students at Carnegie Mellon University (CMU) developed abstraction techniques making possible the efficient verification of pipelined processors. Professor Ed Clarke and students at CMU applied new model checking techniques to out-of-order instruction verification. **Hardware/Software Codesign** - The hardware/software codesign tool and methodology POLIS from Professor Alberto Sangiovanni-Vincentelli at the University of California at Berkeley formed the basis for the Felix codesign tool commercialized by SRC member Cadence Design Systems. A technology transfer course in June 1998 presented the concepts and operation of codesign to an industry audience of semiconductor designers and customers and design automation vendors.

**Verification Interacting with Synthesis** - The Verification Interacting with Synthesis system (VIS 1.3, was released by the University of California at Berkeley, the University of Colorado, and the University of Texas at Austin in September. This is the third release of what has become the de facto standard platform for testing formal verification ideas. The new release, among many other things, adds combinational and sequential synthesis within the VIS framework, forward model checking, and finite state machine restructuring for power reduction. Professor Robert Brayton reports an average of two downloads daily from the Berkeley Web site.

**Automatic Test Pattern Generation** - Testability has been identified as a major issue on increasingly complex designs. The Nemesis 2.2.3 ATPG software from Professors Tracy Larrabee and Joel Ferguson at the University of California at Santa Cruz now has the ability to generate tests for several models of resistive bridging faults. Circuits may include both combinational and sequential elements, as well as tristates. The companion software SPROING 2.0 performs diagnosis for single stuck-at, transition, or bridging faults with only a stuck-at fault dictionary.

**High-Level Power Estimation** - Power management is increasingly important as complexities increase. It is imperative for portable applications as well as to relieve thermal package concerns affecting long-term reliability. Professor Farid Najm and his students at the University of Illinois at Urbana-Champaign have developed macroscopic design methods aimed at power estimation. Prior to design, the top-down method predicts required area and power of circuit blocks using a high-level functional description, delay specification, gate library, and I/O switching activity; the bottom-up method macromodels large circuit blocks based on input switching activity.

**Interconnect Synthesis** - Professor Lawrence Pileggi and his students at CMU are working to develop metrics, methodologies and algorithms to enable accurate, reliable design – both electrical and geometric – of integrated circuit and system interconnect. Progress in 1998 includes (1) development of a new accurate RC-delay model (H-gamma) for interconnect synthesis to replace the long-used, but inaccurate (for deep submicron regime) Elmore RC-delay model, and (2) development of a new accurate, efficient approach for extracting frequency-dependent inductance for interconnect.

# Research Contributions

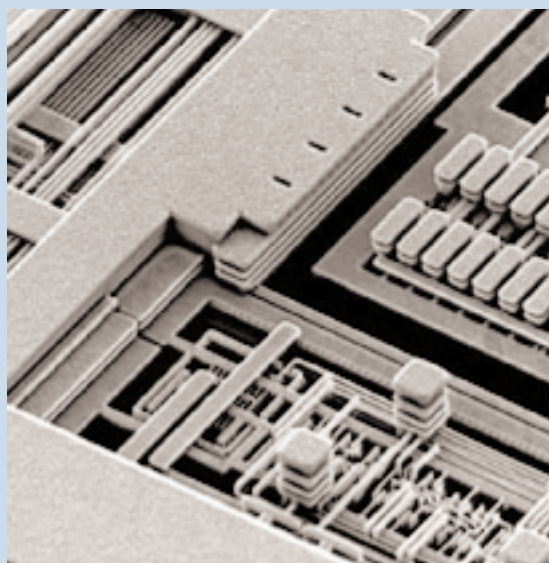


Photo courtesy of IBM Corporation

## Process Integration and Device Science

### **3-D Silicon-on-Insulator (SOI) Technologies Using Epitaxial Lateral Overgrowth (ELO) -**

Integrated Circuits of giga-scale integration and beyond may require that devices be fabricated in multiple levels, i.e., 3-D integration. Stacking devices in 3-D has potential for increasing the density of memories and microprocessors, but could also allow faster parallel processing with computational building blocks. Led by Professor Gerold Neudeck at Purdue University, silicon on insulator (SOI) technologies have been developed using selective epitaxial growth (SEG), epitaxial layer overgrowth (ELO) and Chemical-Mechanical Polishing (CMP) to create device size islands. To achieve 3-D integration, multiple layers of SOI (MLSOI) islands were formed by repeating the process for a single layer. MOSFETs can be placed in both layers of islands. Deep submicron, FD-SOI p-MOSFETs have been fabricated in both layers to demonstrate the device quality of the material in each layer. (Devices have not yet been fabricated in both layers on the same chip.) In addition, This technique provides a 3-D geometry with very smooth interfaces for possible future quantum devices and nanostructures. Material quality is a critical issue in SOI technology. The material fabricated with this SEG/ELO technology is high quality. Islands as small as 150 nm x 150 nm x 40 nm thick and as large as 5 mm x 150 μm x 0.1 μm thick have been fabricated.

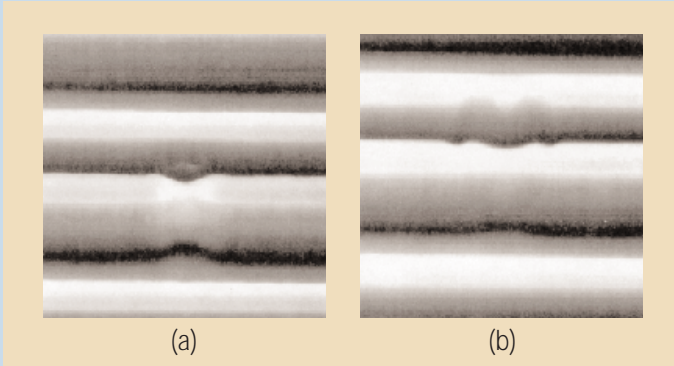
## Factory Sciences

**Feasibility study of a contamination-defect-fault relationship and mapping tool** -Traditional yield-ramping has relied on physical failure analysis to diagnose problems with a manufacturing process. However, physical failure analysis is an expensive, labor-intensive and sometimes unfruitful venture. A faster technique has been developed by Professor W. Maly and his students at CMU which uses electrical test information to perform cost-effective defect diagnosis. The purpose of this study was to examine the feasibility for using this approach to reliably map electrical circuit faults uniquely to the defect causing the fault. A contamination-defect-fault (CDF) relationship is modeled in CODEF, which, given a prescribed process and circuit layout topology, maps a contamination particle into a process defect resulting in a defective circuit. The SPICE circuit of this defective IC segment is then extracted and catalogued. A comparison of a measured circuit fault with a catalogue of simulated faults, each correlated with a known defect, then maps a measured circuit fault uniquely to a known defect. In this study CODEF was used to characterize faults of a SRAM as a test vehicle for Intel's 0.25-μm CMOS process. Fault paretos were generated from simulation data and verified against results from Intel's yield analysis group with focus on process start-up problems during definition of poly lines. The key goal of the study was the identification of both the predominant fault and the most problematic processing step during the process phase. Following substantial CODEF simulations (250,000 simulations with particles evenly distributed among 80 processing steps), a unique fault type list for each of the 80 processing steps was extracted by circuit netlist comparison tool, Gemini-II. The resulting 80 fault-type lists were combined by a final netlist comparison to one large fault-type list. Stacked bar graphs and fault paretos of all processing steps were generated and compared to process startup data. The most problematic processing steps as well as the most frequent SRAM faults were identified successfully and scripts were written to visualize the layout location of particles causing the specific faults.



**Lithography Defect Simulation** - Professor W. Maly and his students at CMU have also collaborated with AMD to apply CMU's 2-D topographical simulation tool, METROPOLE, to the simulation of defects in i-line lithography. In this case, METROPOLE was used to map defect types to faulty photoresist profiles, which formed the basis of a dictionary. This correlation was then used to provide insight into defect mechanisms that cause major distortions in photoresist profiles. The nature of the distorted patterns was used in yield improvement efforts by comparing simulation results with the observed photoresist profiles on wafers. Using this methodology, defect sources were identified and defect densities were dramatically lowered, in one some by a factor of 10X.

*Photographs provided by Advanced Micro Devices, Inc.*



*Specific notching defects in photoresist lines such as shown in (a) and (b) above can now be identified and understood by simulations and then reduced using focused yield improvement efforts.*

## Interconnect Sciences

**Fabrication of Ultra-thin C-Si Polymer Films for Use as Adhesion and Diffusion Barriers in Cu/Low-K Integration** - The introduction of Cu in metallization architectures requires a barrier both to prevent diffusion of Cu into the device material and also to improve Cu adhesion to the dielectric substrate. In order to meet the requirement of 0.1 micron geometries, such films should be capable of consistent processing and performance at thicknesses < 100 Å. Professor Jeff Kelber and his students at the University of North Texas have fabricated C-Si films on Cu and Ta substrates by UV or electron-induced cross-linking of vinyl silane monomers. Films < 100 Å thick have inhibited Cu diffusion to temperatures in excess of 800 K (527 C). Auger studies of Cu deposited onto such films suggest adequate adhesion due to a strength of Cu-substrate chemical interaction comparable to that between Cu and Ta with one

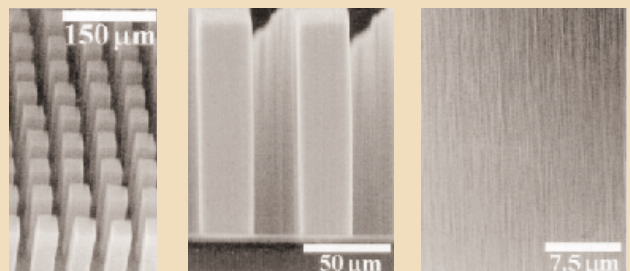
monolayer of oxygen. The films show excellent thermal stability on Cu and Ta, and do not delaminate under thermal cycling. Films formed on Ta do not decompose at temperatures below 1000 K. Films containing only C, Si and H react slowly until O has been stoichiometrically inserted in existing Si-C bonds. This property may afford a mechanism for preparing ultrathin silicon oxycarbide and silicon nitrocarbide films with useful chemical and electronic properties. The chemical structures and properties of the films formed to date suggest an excellent potential as "capping" layers to inhibit Cu diffusion into xerogels and other porous dielectrics with dielectric constants < 2.0.

## Lithography Sciences

**Advanced Resist Research** - Professor Grant Willson and his students at UT-Austin continue to push the extensibility of optical patterning by designing and demonstrating the feasibility of optically printing arrays of 80 nm line/120 nm space pairs with a novel single layer resist and 193 nm phase mask technology. During 4Q98, they also optically printed isolated arrays of 80 nm features using 193 nm radiation, novel top surface imaging materials, and a binary mask. Their results suggest that optical patterning might be extensible through the end of the current NTRS.

**Maskless Patterning** - Professor Calvin Quate and his students at Stanford have patterned rows of deep sub micron features by scanning a linear array of 50 addressable probe tips. Also, Professor Dai at Stanford recently demonstrated a moderately low temperature CVD process for growing dense, patterned, anisotropic brush-like arrays of nanotubes. This emerging control over the synthesis of nanotubes represents a potential breakthrough opportunity with broad applicability beyond patterning.

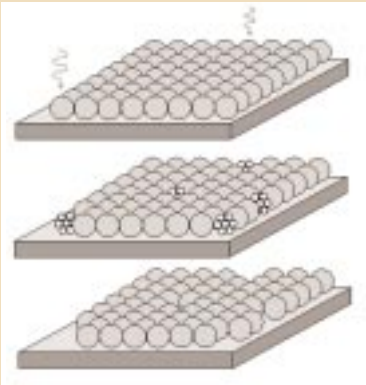
## Patterned Arrays of Nanotubes



*Photographs provided by Professor Hongjie Dai, Stanford University*

**Resist Synthesis and Modeling** - Professor Jean Frechet's team at UC-Berkeley, in collaboration with Professor Quate's group at Stanford, has designed novel resist systems and demonstrated the feasibility of patterning with monolayers of beam sensitive dendrimers. These dendrimers can be engineered to different effective diameters, ~5-8 nm, and can pack in regular arrays on the surface of wafers. The probe beam induced decomposition of a specific dendrimer promises to image nanometer scale openings to the substrate.

### Addressing Individual Molecules



Each sphere is a globular polymeric macromolecule with a diameter of 1-10 nm

Photochemical reactions cause either (a) the decomposition of the macromolecule ...

... or (b) exclusion of the macromolecule from the self-assembled monolayer

### Materials and Bulk Process Sciences

**Modeling of Ion Implantation** - Professor Al Tasch at UT-Austin completed the development and validation of the ultra-low energy model in UT-MARLOWE by making major modifications to the classical binary collision approximation (BCA) theory such that it is applicable at ultra low energies. This new model has been experimentally verified for B and As implants at energies down to 1 and 2 KeV, respectively and model predictions are in good agreement with SIMS data, achieving excellent fits to a variety of SIMS profiles from KeV to MeV energies, and from B to In masses. This will be important in creating ultra-shallow source/drain junctions for CMOS transistors at nodes below 100nm.

**Research on high K gate dielectrics for MOSFETs at Minnesota** - As the MOS transistor continues to scale, better gate dielectrics are needed to obtain required transistor drive characteristics while maintaining sufficient voltage breakdowns and low device leakage, a critical factor for low power designs. Professor Steve Campbell has demonstrated high K films with an equivalent oxide thickness (EOT) of about 1 nm. This research has

attained a significant milestone in the search for a suitable sub- 1 nm high K gate dielectric. This work is important to the re-engineering of the CMOS transistor for nodes below 100 nm.

### Packaging Sciences

**Moire Study of Structural Integrity of High-Density Flip-Chip Packages** - Plastic area-array packages with under-filled flip-chip configuration have become an enabling technology for high-performance and low-cost giga-scale packaging integration. The development of area-array packages incorporates new sets of materials, processes and interconnect structures that are not always optimized and compatible. These issues can give rise to serious manufacturing and reliability problems as the package types enter production. Structural integrity is of particular concern due to thermal deformation caused by the mismatch in thermal and mechanical properties of the packaging materials and the silicon. The development of phase-shift Moire interferometry led by Professor Paul Ho at UT-Austin has provided a high-resolution capability for direct measurement of the stress-strain distribution in flip-chip

packages. Using a phase shift technique, the interferometer has demonstrated a resolution of 26 nm for structures as small as 25 microns. This is a 16x improvement over standard Moire interferometry, extending the technique for studying chip-to-packaging interconnects for future generations. The results were used for direct assessment of the structural integrity and experimental verification for computer modeling, which, in turn, provided feedback for design optimization and processing improvement. In collaboration with member companies, this technology is being applied for packaging development of Cu/low k interconnects.

### Environmental Safety and Health

**Resist Research** - Professor Chris Ober and his students at Cornell University have designed new families of resist materials that can be patterned with an environmentally benign, closed loop, supercritical CO<sub>2</sub> development process. This process is analogous to that used for decaffeinating millions of pounds of coffee annually and would create little or no developer waste. During 1998, this team demonstrated the feasibility of patterning arrays of 200 nm line/space pairs.

## Supercritical CO<sub>2</sub> Development of Photoresists

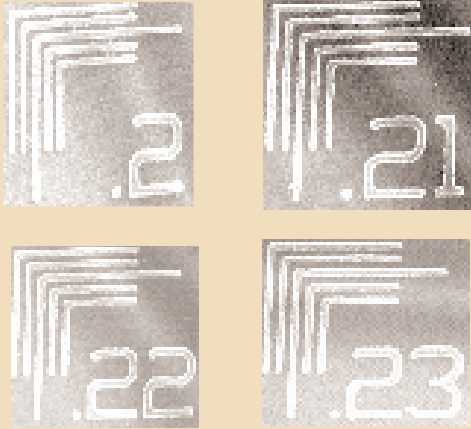


Image with 191 nm Source

Photograph provided by Professor Chris Ober, Cornell University

## Metrology

### Ultra-low Voltage Electron Beam Imaging -

The detection and identification of circuit defects as small as a few nanometers becomes critically important as feature sizes shrink to those dimensions. Professor David Joy's research team at the University of Tennessee-Knoxville has developed new approaches to metrology using ultra-low voltage electron beam spectroscopy [1-100 eV] and has demonstrated the feasibility of resolving gross composition defects on the nanometer scale and at high speed. The ultra-low energy beam eliminates damage and contamination concerns. The initial demonstration using an Auger spectrometer with a 10 nm probe size demonstrated a count rate about  $10^6$  higher than expected for X-ray analysis. Spectra can be recorded in a very short time with good signal to noise ratio.

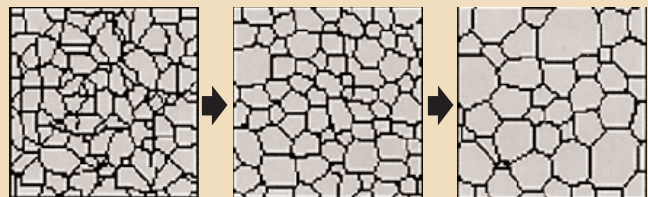
**Development of High Resolution (10 ns/100 nm) Thermometry for Devices, Interconnects, and Packages** - As feature sizes shrink and circuits operate at higher frequencies, the ability to measure temperature with high spatial and temporal resolution becomes more important. Highly localized temperature excursions are having a greater and greater influence on the performance and reliability of devices (e.g., SOI MOSFETs), interconnects (e.g., ESD events in thin metal lines), and packages (e.g., at flip chip, CSP, and BGA interfaces). In addition, novel methods with high resolution are required to characterize the thermal properties of the new thin films being introduced at all levels of circuit manufacturing. Professor Kenneth Goodson and his students

at Stanford have developed a unique thermometry capability that provides the spatial and temporal resolution required to study and characterize all of these phenomena. The system employs optical reflectance in both the far-field and near-field regimes as the thermal probe. The far-field regime is used to look at structures with dimensions as small as 500 nm and the near field for structures with dimensions as small as 100 nm. The time resolution is 10 ns or less. Work is now under way that uses this unique tool for better understanding and improved modeling of the thermal properties of SOI devices, ESD phenomena, packaging interfaces and thin films.

## Semiconductor Modeling and Simulation

The fourth year of the SRC's CRADA on Semiconductor Modeling and Simulation involving 10 SRC member companies, 10 universities, Los Alamos National Laboratory and Sandia National Laboratory was extremely productive. The CRADA thrusts are: Bulk Processes, Gridding Technologies, Materials Reliability and Topography. One of the CRADA projects is focused on the development and validation of a physically-based reliability estimation tool for VLSI interconnect systems. This project involves collaboration between the National Laboratory scientists, led by Dr. Galen Straub of LANL, Professor Carl Thompson of MIT, and Professor Harold Frost of Dartmouth College. The team is working to extend 2-D interconnect predictive reliability tools developed at the universities to handle 3-D structures with appropriate representation of interconnect sidewall effects. In 1998, excellent progress was made on interconnect metal grain growth for use in electromigration reliability computations. The sophisticated grid technology, LaGrit, developed by the National Laboratories, was used for 3-D models of dynamic grain structure motion and shape evolution under excitation.

## Polycrystalline Film Evolution with Annealing



### Grain Growth to Stagnation

- Driving Forces for Grain Growth
  - Grain boundary energy reduction
  - Surface, interface and strain energy minimization

Photograph provided by Dr. David Cartwright, Los Alamos National Laboratory

# SRC Restructures

## SRC Restructures in 1999 to Optimize Member Value

*The structure of the industry SRC series is changing as we approach the 21st century; for example, more equipment suppliers are also becoming process providers, CAD companies increasingly offer design services, the number of fabless IC companies is growing and SRC members are directing efforts to their core DSP, Telecommunications and Microprocessor businesses.*

By moving to fewer science areas (seven areas are reduced to four in the new structure) the change favorably positions SRC to:

- **attract new members from the equipment supplier and fabless IC industries.** New members may participate as Science Area members with dues scaled to their actual areas of interest. Equipment and materials suppliers will find value as Material and Process Sciences members; CAD companies as Computer-Aided Design and Test Sciences members. Science Area members have access to the entire SRC portfolio.
- **encourage effective and efficient member involvement in a broad-based cross-disciplinary planning effort.** Strategic Planning occurs at the Science Area level. Each member company may assign representatives to the four Science Area Coordinating Committees, who oversee strategic and planning efforts. Although they may assign a representative to any or all of the eight related Thrust Technical Advisory Boards, members who choose to limit their representatives to specific thrust areas can still engage in the full spectrum of planning activities through their Coordinating Committee representatives.

### The four new science areas are:

#### Computer-Aided Design and Test Sciences (CADTS)

The challenges of supporting the design of a billion transistor chips and systems will require unprecedented advances in design tools at many levels and in test methodologies. CADTS research spans physical design, synthesis, verification and test for digital and mixed-signal systems. CADTS seeks to develop innovative approaches to increased design productivity in response to the needs of members and also contributes to new product concepts for the CAD industry.

#### Integrated Circuits and Systems Sciences (ICSS)

This new science area is designed to address the growing design needs of members and to attract new members from the design services industry and from the fabless integrated circuit industry. ICSS will focus on new circuit and system design methodologies and concepts to serve the members for whom integrated design solutions are critical to competitiveness.

#### Materials and Process Sciences (MPS)

In order to meet the performance requirements for future generation integrated circuits, the semiconductor industry must re-engineer the MOSFET, it must employ patterning systems providing sub 100 nm feature sizes, and it must address the limitations imposed by known metal and insulator interconnect systems. MPS is designed to provide a synergistic approach to the resolution of challenges by comprehending materials and process research in device, interconnect, patterning, and environmental safety and health technologies.

#### Nanostructure and Integration Sciences (NIS)

The idea of technology integration is central to this new science area at the chip, package and factory levels. NIS seeks new devices realized by integrated processes to satisfy transistor needs in the 2010 time frame. NIS also conducts research on advanced package technologies that are central to the realization of integrated systems, and it takes an integrated view of the operation of the factory as a system whose performance is to be optimized.

Synergistic to the four science areas, a special Cross-disciplinary Semiconductor Research (CSR) program encourages initiatives for high-risk research that may lead to breakthrough or disruptive technologies addressing the long-term needs of the industry. CSR provides one year exploratory funding for cross-disciplinary teams to develop proposals for support from one or more of the SRC science areas. It is one way SRC attempts to tap innovation and promote revolutionary approaches to addressing the next generation of IC challenges.



# Value Management Programs

## Value Management Programs

In 1998, the scope of the SRC Technology Transfer Group was formally extended to address the entire value chain – including the creation, delivery, extraction and advocacy of value stemming from the SRC research agenda and results. Accordingly, the Technology Transfer Technical Advisory Board (TTTAB) was renamed the Value Chain Technical Advisory Board (VCTAB) and their responsibilities were expanded and documented.

## A Focus on Information Quality

During this transitional year, much of the operational activity needed to support the identification, storing and distribution of research information was formally placed under the Value Management umbrella. The Value Management team, in conjunction with SRC staff, assures the quality of this information so that it can be extracted monthly to the member-secure area of the SRC Web site.

## Team-Driven Achievements

Key accomplishments were guided by two VCTAB subteams established in 1998: Effectiveness and TECHCON Marketing. The Effectiveness team targeted the implementation of industry and university recommendations made at the 1997 Summer Study. Site review pre-reading materials describing key research accomplishments, subsequent year's plans, and technology transfer highlights were delivered to Technical Advisory Board members attending the review. At the request of industry, research proposals were posted to the SRC Web site for Advisory Board access. Additionally, TAB members reviewing research proposals are now provided a summary of the technical recommendations made to investigators at the annual site review – the purpose is to provide a framework for evaluating the proposal.

Under the guidance of the Marketing sub-team, a distributed electronic approach to publicity for TECHCON'98, allowed SRC to eliminate over \$20,000 in production and mailing costs. The approach allowed delivery of member-customizable, concise, targeted information about the conference in formats suitable for e-mail and posting to the SRC and member internal Web sites.



Three panel sessions at TECHCON '98, were coordinated by the Value Management Team. Dinesh Mehta of SRC moderated a session entitled *SIA/SRC/SEMATECH/MARCO: Addressing the NTRS Grand Challenges*, which was designed to encourage creative approaches to addressing the critical 'red' areas of the NTRS. A session on *Strategic Workforce Issues* was moderated by Professor Mark Law of the University of Florida. A third session on *10 Ways to Simplify Working with SRC* was moderated by Gail Massari of SRC.



*Ken Ports, VCTAB Chair from Harris Semiconductor challenges the VCTAB to address improved processes that assure maximum member value – from planning through technology diffusion.*

# Student Relations

*1998 saw the growth of established student programs and much effort spent on starting two new initiatives: a pilot program of SRC Undergraduate Research Scholarships and creation of a Human Resource Needs Roadmap. Going forward, the careful integration of established programs and new initiatives will ensure a broader scope for SRC Student Relations.*

## 1998 Accomplishments

- 779 students were supported under SRC contract research providing an outstanding source of technology transfer through internships and permanent hire.
  - Of 139 graduating students, 75 were hired by SRC member organizations/universities, representing 54% of the graduating population. A value model for student hires was developed by the Student Relations TAB to assist members in defining the value derived through student hires.
  - 55 Fellowships were supported under the Graduate Fellowship Program. Of the 10 Fellows completing the GFP in 1998, 6 joined member companies or university faculties.
  - 14 company-named fellowships were in place during 1998 as follows: AMD, 3; Harris, 1; IBM, 2; Motorola, 4; National, 2; Texas Instruments, 2.
  - 9 Master's Scholarships were supported, four continuing from 1997 and 5 beginning in the fall of 1998.
  - Access to and information about SRC students was enhanced in 1998 by increasing the number of student resumes available on the Web site, enhancing search capability and providing a web-based spreadsheet of students looking for internships.
- 236 SRC students presented their research at TECHCON '98.
  - 20 SRC companies participated in JobsFair at TECHCON '98.
  - The GFP Annual Conference Banquet was held at TECHCON '98 and the Fellows Award for "Outstanding Research Presentation" was presented to Dennis Sylvester, University of California at Berkeley.

## New Directions

- A program of Undergraduate Research Scholarships was successfully piloted during 1998 with 9 summer scholarships and 2 academic year scholarships placed through SRC-funded faculty. A small number of scholarships will be awarded for the summer of 1999 as funds allow.
- SRC accepted responsibility for the Engineers/University segment of a Human Resource Needs Roadmap at the request of the SIA and with support and direction from the SRC Board of Directors. The Roadmap document, largely completed in 1998, includes a needs assessment and gap analysis for technical human resource for the semiconductor industry into the 21st century. This document will guide much of the work of Student Relations in 1999.



*SRC Fellows at TECHCON '98. New SRC Fellow, Stefan Riege from MIT, explains his research to Jean Kelsey who will complete her doctoral study at SUNY/Albany as an SRC Fellow in 1999 and join IBM Corporation.*



# Aristotle Award Presented at GFP Conference

Two Aristotle Awards were presented in 1998 recognizing excellence in teaching through the research process. The awards were presented at the Graduate Fellowship Program Annual Conference at TECHCON '98 in Las Vegas, NV, to Professors Franco Cerrina and Joseph Greene.

**Professor Cerrina** directs the Center for X-ray Lithography at the University of Wisconsin-Madison. His former students speak of his ability as a scientist and researcher that has made him a leader in his field and the affect that has had on their own development as graduate students. Through Professor Cerrina's leadership, dedication and hard work, the Center for X-ray Lithography at the University of Wisconsin has been molded into one of the world's leading research centers in the area of advanced lithography, producing graduate students with skills and background that allow immediate contribution to the semiconductor industry.

**Professor Greene** is well known for providing an atmosphere in which outstanding students can produce outstanding accomplishments. He teaches his students to be good citizens in the scientific community by encouraging their early participation in professional societies. His students attribute the success of Professor Greene's research in great measure to the team spirit of the group. Students are expected to work together for the benefit of the group, and they are expected to understand all aspects of the research well enough to challenge each other's ideas. In his tenure at the University of Illinois, Professor Greene has graduated 34 doctoral and nine master's students; four SRC Fellows are among his current and past students.



## GFP Fellows

**Andrew Abo**  
University of California at Berkeley

**Peter Abramowitz**  
University of Texas at Austin

**Michael Beattie, Texas Instruments/SRC Fellow**  
Carnegie Mellon University

**Michael Booth**  
Cornell University

**Christopher Borst**  
Rensselaer Polytechnic Institute

**Arthur Bradley\***  
Auburn University

**Scott Bukofsky\***  
Yale University

**Danny Chen**  
Cornell University

**Jir-Shyr Chen, IBM/SRC Fellow**  
Cornell University

**Paul Dentinger\***  
University of Wisconsin

**Jonathan Doan**  
Stanford University

**Joe Fenner, Robert M. Burger Fellow**  
North Carolina State University

**Timothy Fisher\***  
Cornell University

**Brian Floyd, Harris/SRC Fellow**  
University of Florida

**David Fryer, Texas Instruments/SRC Fellow**  
University of Wisconsin

**Glenn Glass, Motorola/SRC Fellow**  
University of Illinois

**Heidi Gundlach**  
University at Albany, State University of New York

**Jennifer Havard, AMD/SRC Fellow\***  
Cornell University

**Noel Hoilien**  
University of Minnesota

**Gregg Hoyer**  
University of Washington

**Anna Ison, Motorola/SRC Fellow**  
University of California at Berkeley

**Maura Jenkins**  
Stanford University

**Simon Karecki, Motorola/SRC Fellow**  
Massachusetts Institute of Technology

**Norman Kay**  
University of Arizona

**Jean Kelsey**  
University at Albany, State University of New York

**Michael Krasnicki**  
Carnegie Mellon University

**Jae-Wook Lee**  
University of California at Berkeley

**Steven W. Levine\***  
Cornell University

**Aaron Lilak**  
University of Florida

**Derek Martin**  
University of Florida

**George McMurray**  
University of California at Berkeley

**Katherine Mueller\***  
University of Texas at Austin

**James O. Keffe**  
Stanford University

**Michael Orshansky, AMD/SRC Fellow**  
University of California/Berkeley

**Shipra Panda, NSC/SRC Fellow**  
Carnegie Mellon University

**Michael Perkins, NIST/SRC Fellow**  
Stanford University

**Laura Purette, Motorola/SRC Fellow**  
Massachusetts Institute of Technology

**Sriram Rajamani**  
University of California at Berkeley

**Benjamin Rathsack, NSC/SRC Fellow**  
University of Texas at Austin

**Stefan Riege**  
Massachusetts Institute of Technology

**Lance Robertson, IBM/SRC Fellow**  
University of Florida

**Eric Shero\***  
University of Arizona

**Brad Shutzberg**  
Cornell University

**Jeffrey Snodgrass**  
Stanford University

**Robert Sumners, AMD/SRC Fellow**  
University of Texas at Austin

**Dennis Sylvester**  
University of California at Berkeley

**Bassam Tabbara**  
University of California at Berkeley

**Nerissa Taylor**  
University of Illinois at Urbana-Champaign

**Robert Thacker**  
University of Utah

**Shawn Thomas**  
University of California at Los Angeles

**Peter VanDerVoorn\***  
Cornell University

**Andy Wei**  
Massachusetts Institute of Technology

**Chad Weintraub**  
North Carolina State University

**Heidi Witschi**  
University of Wisconsin

**Xin Yi Zhang**  
Stanford University

## Master's Scholars

**Paul Ampadav**  
University of Washington

**Adreanne Kelly**  
Lehigh University

**Ronald Kinder**  
University of Illinois

**Francisco Machuca**  
Stanford University

**Toussaint Myricks**  
University of Washington

**Adrain Robinson**  
Rensselaer Institute of Technology

**Tamara Tubbs**  
Georgia Institute of Technology

**Jaimal Williamson**  
Georgia Institute of Technology

**Enrique Valesco**  
Stanford University

\*Graduated in 1998

# Technical Excellence Award

*Recognizing Research That Accelerates Innovation*

*Since its inception 1991, the SRC Technical Excellence Award has recognized 48 researchers and 14 major research efforts whose technological contributions have significantly enhanced the productivity of the U.S. semiconductor industry. Each year a research team is chosen based on the team's creativity and innovation, scientific merit of their research, value to industry of the results and effectiveness of the team at technology transfer.*

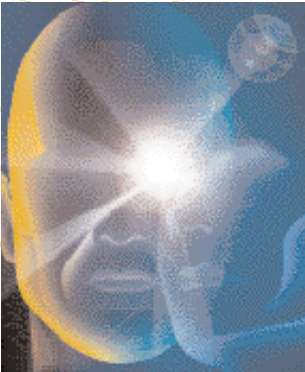
The 1997 Technical Excellence Award was presented to Professor William Oldham, Dr. Richard Schenker and Mr. Fan Piao for their outstanding research at the University of California at Berkeley on "Ultraviolet Damage to Fused Silica." Their work involved innovative research on new methods of measuring optical materials compaction and the effects of damage on lithographic performance for the 193 nm regime. Prior to this work, data on damage to fused silica at 193 nm was either unavailable or poorly organized. Therefore, it was nearly impossible to assess the difficulty of 193 nm material technology implementation or its likelihood of success. Given the impending need for smaller lithographic resolution, this created a research dilemma for both users of lithographic exposure equipment and manufacturers.

The information supplied by the UCB team provided key information on the state of 193 nm technology and facilitated cooperative interaction with the suppliers of semiconductor equipment. Due to the extensive and high quality publications produced by the research team, the results were simple to implement and easily comprehended. The research team was completely open in disclosing both successes and problems encountered throughout the program. It is estimated that the pace of technology implementation has been accelerated by 3-5 years based on the team's efforts which have made a major impact in our understanding of DUV optical materials.



*(L-R) Dr. Richard Schenker, Professor William Oldham and Mr. Fan Piao display their commemorative awards as recipients of SRC's Technical Excellence Award at TECHCON '98.*

# Industrial Liaison Program



The SRC Industrial Liaison Program was launched in 1983 (as the Mentor Program) to provide a formal framework for human interactions that stimulate creativity and solve technical challenges. SRC Industrial Liaisons are over 500 scientists, engineers, and managers from SRC member companies who are interested in supporting specific research tasks and actively managing and planning for the desired program results. They provide three critical functions as part of the SRC-University-Industry team: Research Facilitation; Technology Transfer; Student Mentoring.

The SRC community recognizes the significant contributions of Industrial Liaisons with an annual award. Six winners for the 1998 Award were chosen from among the university and industry nominations.



Robert Aitken

**Robert Aitken** of *Hewlett Packard* worked with Professor Tracy Larrabee and student, David Lavo (now of Hewlett Packard), at the University of California, Santa Cruz. Professor Larrabee said "I think of this relationship as the very best that SRC mentorship has to offer to both the academic research program and the industrial partner."



Laurie Beu

**Laurie Beu** of *Motorola* worked with Professor Rafael Reif of MIT. Ms. Beu was outstanding in her commitment to ensure that Professor Reif's work in plasma etching stays at the forefront of the industry. Ms. Beu promoted the project to other companies, opening the door to collaborations with gas vendors and equipment manufacturers.



Martin Giles

**Martin Giles** of *Intel* worked with Professor Mark Law at the University of Florida. According to Professor Law, there is a constant tension between asking universities for fundamentally new knowledge while requesting a constant stream of short-term deliverables that are useful to industry. Dr. Giles' approach illustrates that industrial mentors can help SRC reach both goals.



Effiong Ibok

**Effiong Ibok** of *Advanced Micro Devices* worked with Professors Wortman and Hauser at North Carolina State University. Dr. Ibok provided test chips and process technology information, maintained regular discussions with Professors Hauser and Wortman, and arranged training and instructional programs for AMD engineering staff on the use of NCSU's electrical characterization method.



Sungho Jin

**Sungho Jin** of *Lucent Technologies* is recognized for his work with Leon Keer's research on interface reliability studies at Northwestern University. He encouraged ingenuity, innovation and the use of every available resource to achieve research goals. Dr. Jin also provided valuable feedback on the significance of the research in meeting industrial needs.



Alexander Liddle

**Alexander Liddle** of *Lucent Technologies* worked with Professor Roxann Englestad at the University of Wisconsin, Madison. Three students wrote of him, "It has been inspiring to meet a scientist with such technical expertise that also has a sense of humor, integrity and honest consideration for the people with whom he works."

# SRC Web Site – The Next Generation

*Delivering Value in Information: SRC Web site - The Next Generation SRC Web site has been dramatically expanded in 1998 to better support the SRC community. It was redesigned to improve the integration of information about SRC and its programs into the daily workflow of personnel that can contribute to and gain value from it.*

## The Challenge

The challenge faced by SRC's Web architects was two-fold: to substantially improve value delivery and to integrate and manage extensible information and technology strategies targeted to meet the increasingly more sophisticated and complex set of user requirements. It was equally clear that this was far more than the application of information technologies.

## An Expanded Architecture

To accommodate the ever-growing volume, complexity and usage of information, the site architecture had to be scalable and extensible allowing rapid response to new and changing requirements. This was tackled by addressing both the information system technologies employed and the information management processes in place at SRC that collect and manage data. Efforts focused on business processes, data models, implementation methods and quality initiatives to ensure timely and accurate information capture, management and delivery.

## New and Improved Site Design

From a user's perspective, the most obvious site improvement is a completely redesigned look and feel. With over 12,000 pages of content, it was imperative that a more robust methodology be found for easily navigating the site. The first major step toward this goal was an innovative expanding and collapsing menu structure that remains onscreen and readily accessible throughout the site.

## Features

As site content grew, it became increasingly more important to make users aware of timely new content without forcing them to scroll or scan through a long list of links or search functions. Using a newspaper paradigm, SRC adopted a "Features" column on the home page that presents the latest headlines of SRC and each one is just a click away from the home page.

## New and Improved Search

Of course, with any large Web site, there is always a need for a robust search capability. SRC greatly enhanced the site search engine in three areas. First, the Search function is now always prominently displayed in the top banner of the SRC site regardless of location. Second, an advanced Search capability was implemented that provides a far more robust set of capabilities within subsets of the site. Finally, Search now integrates all site content including the full content of all documents in Portable Document Format (PDF).

## Secure Content

General information about SRC is available to the public without requiring a login, but the vast majority of content on the Web site is available to personnel at member companies or current researchers via privileged user accounts that require login. Until a user logs in, this content appears "locked" and attempts to access it simply yield a login information screen.

## User Profiling

Unlike newsletters or email, a Web site requires that a user initiate a request for information at the Web site. In this busy world, it would be advantageous to know when something of specific interest to you became available. Starting in 1998, SRC deployed the first phase of its user profiling capability.

## Not Just About Delivery

While the success of the World Wide Web is founded on rapid access to information, the Web can also provide a ready means to collect information from users while maintaining a high degree of integrity and reliability in the information received. Numerous "forms" now exist on the SRC site that enable rapid collection of data and member participation.

## What the Future Holds

SRC will continue to update its Web site consistent with the growth and capability of the Web and the needs of the SRC community.



# MARCO's Focus Center Research Program

*The Microelectronics Advanced Research Corporation (MARCO) is a wholly owned but separately managed subsidiary of SRC. MARCO is a not-for-profit research management organization that can manage research projects for individual customers or consortia. At the present time MARCO is managing the Focus Center Research Program (FCRP) for a consortia including semiconductor device manufacturers, and their equipment and material suppliers. The Department of Defense is a co-participant in this program, with their management being provided by DARPA. Two Focus Centers were launched in 1998, with four additional Focus Centers anticipated to be started in the near future.*

Research funded by the FCRP is longer range (typically more than eight years out) than that funded by SRC. Although both SRC and MARCO fund work that addresses the challenges of the National Technology Roadmap for Semiconductors (NTRS), FCRP efforts are expected to be multi-university with strong emphasis on cross-fertilization of ideas during the basic research stage. The results of the FCRP are intended to be new concepts and radical alternatives to existing methodologies that address the challenges of the end of the NTRS and beyond.

Basic research advances made as part of FCRP programs may spawn proposals to SRC for research that addresses NTRS needs five years out and beyond. Such research, as it in turn yields results pertinent to solving industrial development challenges, may be identified by the SRC Technical Advisory Boards and industrial constituencies as possible targets for transfer to SEMATECH or third-parties for commercialization.

The organization of the FCRP is made up of funding agencies, program management, lead universities, and affiliated universities. The funding agents are the semiconductor device manufacturers, represented by the Semiconductor Industry Association (SIA), their material and equipment suppliers represented by SEMI/SEMATECH, and the Department of Defense represented by DARPA. MARCO and DARPA manage the FCRP under the direction of a Governing Council made up of representatives from the funding agencies. The technical

and organizational leadership for each Focus Center is provided by a University Director at a lead university. Each Focus Center has a number of affiliated universities, each with one or more associated researchers.

At the present time the FCRP manages two Focus Centers – one in Design and Test with lead university the University of California at Berkeley, and one in Interconnect with lead university the Georgia Institute of Technology. The Design and Test Focus Center presently has nine affiliated universities, the

Interconnect Focus Center presently has six affiliated universities.

The first two Focus Centers will be funded for a two-year period, and then evaluated for progress towards the Focus Center goals. Since two years is a short time to expect significant progress in generating new concepts and radical alternatives to current methodology, the initial evaluation during these two years will be primarily on the process, rather than on results. The two year evaluation will encompass progress in areas such as: generating a widely accepted long range vision for the Focus Center; communication and synergistic performance among researchers in the Center; the availability of a nurturing environment for new concepts and radical alternatives; and the acceptance and support of the sponsoring companies for the Focus Center concept.



# Intellectual Property Report

*Preserving Options for the Future*

Another value of SRC membership is protection of technology and intellectual property assets that are developed as a result of SRC support. SRC has a worldwide, nontransferable, royalty-free, non-exclusive license right to inventions and works of authorship (e.g., software) resulting from SRC-funded research. SRC sub-licenses such inventions and works of authorship, as appropriate, to SRC Members.

U.S. Patents which issued in 1998 included additions to existing technology portfolios in the areas of electromigration, design techniques for circuit reliability, alternative device structures, metrology tools, materials and processes.

Overall, SRC added six newly issued U.S. Patents to its intellectual property portfolio, bringing the SRC's total number of issued U.S. Patents to 156. The table on this page lists SRC U.S. Patents issued in 1998.

## 1998 U.S. Patents Issued

Title	Inventor	Issued	Patent No.	University
Passivated Copper Conductor Layers for Microelectronic Applications and Method of Manufacturing Same	William A. Lanford, Wei Wang, Peijun Ding	6/16/98	5,766,379	SUNY/Albany
Delta Doped and Counter Doped Dynamic Threshold Voltage MOSFET for Ultra-Low Voltage Operation	Chenming Hu, Hsing-Jen Wann	7/14/98	5,780,899	UC/Berkeley
Methods, Apparatus and Computer Program Products for Synthesizing Integrated Circuits with Electrostatic Discharge Capability and Correcting Ground Rules Faults Therein	Sung-Mo Steve Kang, Charvaka Duwury, Carlos Hernando Diaz, Sridhar Ramaswarny	8/18/98	5,796,638	UIUC
Methods, Apparatus and Computer Program Products for Self-Calibrating Two-Dimensional Metrology Stages	Jun Ye, R. Fabian Wedgewood Pease, Michael T. Takac	8/25/98	5,798,947	Stanford
Systems, Methods and Computer Program Products for Prediction of Defect-Related Failures in Integrated Circuits	Mohamed S. Moosa, Kelvin F. Poole	10/13/98	5,822,218	Clemson
Methods of Forming Polycrystalline Semiconductor Waveguides for Optoelectronic Integrated Circuit, and Devices Formed Thereby	James S. Foresi, Anu M. Agarwal, Marcie R. Black, Debra M. Koker, Lionel C. Kimerling	11/24/98	5,841,931	MIT



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